Design and Simulation of group III-V Gate All around MOSFET

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***Abstract*— As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise. A short-channel effect is an effect whereby a MOSFET in which the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction, behaves differently from other MOSFETs. The short-channel effects are attributed to the limitation imposed on electron drift characteristics in the channel, the modification of the threshold voltage due to the shortening channel length. In this paper, a 3-D model of GATE ALL AROUND MOSFET with different gate materials of group III-V (InGaAs, GaAs, InP) is analyzed and comparative study of electrical characteristics of GATE ALL AROUND MOSFETs has been done.**

***Keywords*— GAA MOSFET, Short Channel Effect, Gate leakage, High-k materials, gate.**

I. INTRODUCTION

The revolution in the research of solid-state electronics in general and semiconductor device based electronic industry was started with the development of bipolar transistor, which is found one of the most revolutionary inventions of the 20th Century. In the past years, this invention has been showed an unprecedented impact on the development of the semiconductor science and technology. The Bipolar transistor Shows delay nature when turn on and turn off and also Shows large base-storage times which limit it for high frequency switching application .So, the BJT has replaced by the CMOS technology in the design of digital integrated circuits.

For the past 50 years, relentless focus on Moore's Law transistor scaling has provided ever increasing transistor performance and density. For much of that time, Moore's Law transistor scaling meant scaling where oxide thickness (T_{ox}), transistor length (L_g) and transistor width (W) were scaled. In recent years, CMOS scaling has become less influential in Moore's Law scaling. For generations after the 130nm node (90nm, 65nm, 45nm, 32nm, 28nm) performance enhancers have been added to continue to drive the transistor roadmap forward.

The designing methodologies of modern ICs are established on the CMOS technology. The term "CMOS" refers to both a specific style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips).

Devices with group III-V channels are attractive for increasing speed performance and decreasing power waste over mainstream logic devices using complementary MOS circuitry based on silicon channels. However, III-V devices suffer from short-channel effects such as poor values of off-state leakage, subthreshold slope, and drain-induced barrier lowering. These effects can be suppressed by using three-dimensional structures such as FinFETs and multi-gate formations. The ultimate structure in this trend is to have the channel surrounded by the gate electrode, giving the GAA device. Gate All Around FinFET is a promising candidate because of its quasi-planar structure, excellent roll-off character ristics, drive current and they are close to their root, in terms of layout and fabrication as that of conventional MOSFET. FinFET devices are explicitly mentioned in the ITRS roadmap and have a good potential for scaling CMOS to 45 nm and below**.** The distinct advantages of FinFET are,

- Reduced channel and gate leakage currents.
- High di-electric constant materials is used in order to overcome tunneling.

II. GATE ALL AROUND MOSFET

the gate-all-around (GAA) MOSFETs in which the gate oxide and the gate electrodes wrap around the channel region exhibit excellent trans conductance and short-channel behaviour because of the presence of two additional inversion channels and the occurrence of the strong volume inversion in the MOSFET.

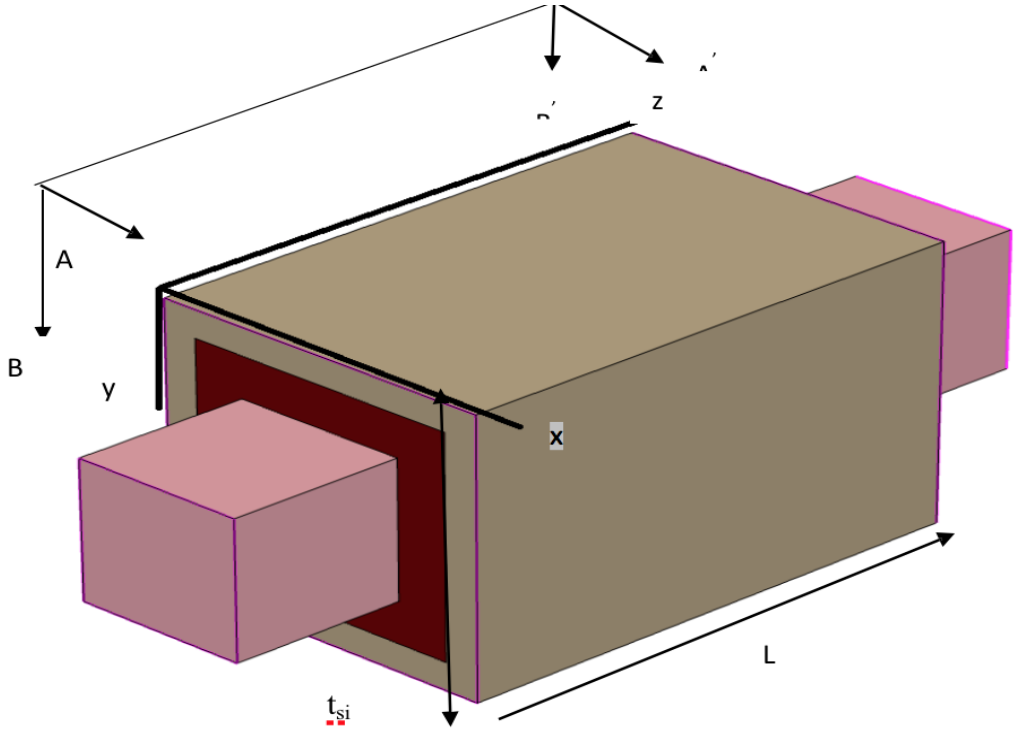

Figure 1: Gate All Around MOSFET

Multi-gate devices, such as, FinFET, Gate-all-around transistors (GAA-FET) improve 3D electrostatic control of the channel. Using GAA MOSFETs can lead to the increase of the ratio of the fin width to the gate length. If the design parameters of GAA MOSFETs are optimized, it is expected that the short-channel effects are adequately suppressed even if the fin width is larger than the gate length. The GAA-FETs are of smaller dimension as compare to bulk type. The body is undoped in this type MOSFETs it enhances the electrical characteristics like mobility ion transfer and removes the drawback which were present in conventional model**.**

III. DEVICE DESIGN AND SIMULATION

In this paper 45nm Gate all around FinFET device are designed for Group III-V Gate materials (relative dielectric > 4). Here InGaAs, InP as gate material. The implementation of high-k materials in the GAA MOSFETs improves the scalability and performance.

Table 1: Specifications of High-k dielectrics

	SiO2	Al2O3	HfO2	ZrO2	TiO2
relative dielectric	3.90	9	25	24	80
thermal conductivity (W/mk)	1.38E+00	2.80E+01	2.20E+01	2.00E+00	7.4
electrical conductivity (S/m)	1.00E-15	1.00E-17	1.00E-12	3.16E-11	1.00E-13
specific heat (J/kg K)	7.09E+02	7.96E+02	2.61E+02	4.50E+02	6.90E+02
density (kg/m3)	2.20E+03	3.90E+03	9.68E+03	5.68E+03	4.95E+03

As shown in Fig.1 the source, drain made up of silicon material and gate is of InGaAs material. While using InGaAs as gate material it reduces the tunneling current through base and increase the current from source to drain. Since the gates are independent, it provides a better control in the variation of threshold voltage can be obtained. Relatively high dielectric materials have higher energy band gap, so that current leakage will be

minimum in the MOSFETs with high dielectric material as its gate material. This leakage current can be further reduced in Gate All Around MOSFETs as the gate fully covers the channel area all along its length, breadth and width.

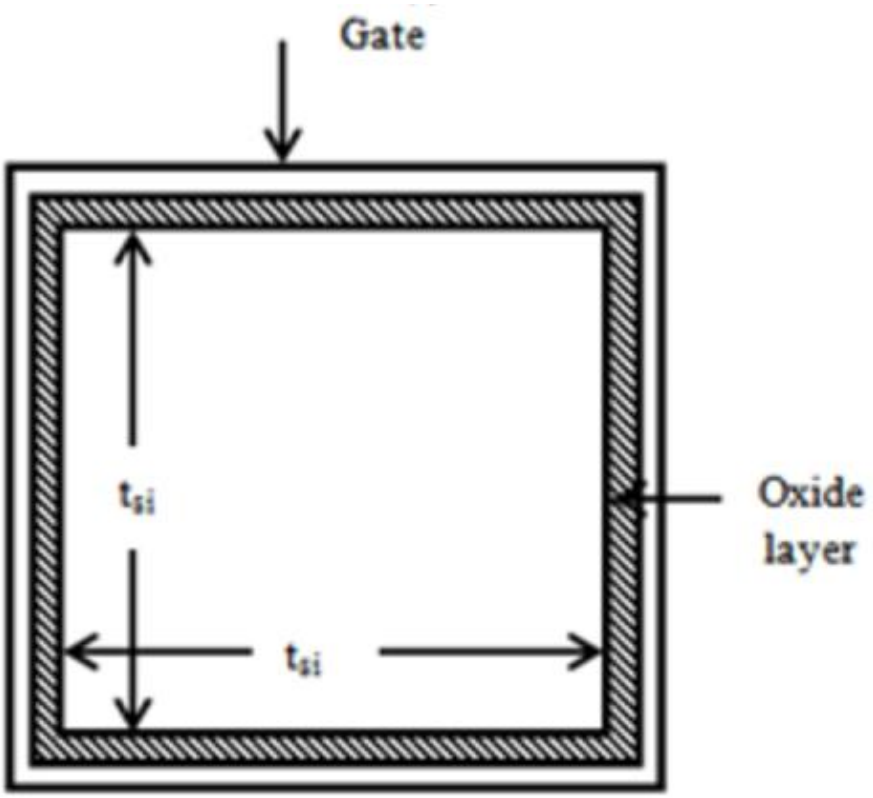

Figure 2: Side View of GAA MOSFET

Figure 2 shows the side view of the Gate All Around mosfet. In this figure we can see the Gate arrangement of the MOSFET all around the channel. High-k material provides good electrical stability, and the amount of charge trapped in the high-k materials remain at a low level even after extended operation of a transistor. It should also be scalable, that provide an acceptable level of leakage and acceptable levels of electron and hole mobility at a reduced thickness. High-k materials satisfying these conditions may be advantageously employed for high performance semiconductor devices.

Since Off current increases, further reduction of thickness of gate oxide material in MOSFET. So an alternative method to increase gate capacitance is altering the relative dielectric constant of the material by replacing silicon dioxide with a high-k dielectric material. In such a scenario, a thicker gate layer might be used which can reduce the Off current flowing through the structure.

IV. RESULTS AND DISCUSSION

The electrical characteristics of GAA MOSFETs were simulated using the open source 3DCC TCAD and lumerical simulator. The device parameters are: channel length L = 45nm, silicon thickness t_{Si} = 30nm, equivalent gate oxide thickness t_{ox} = 2nm, L_{sd} = 50nm, doping concentration of the silicon channel NA = 10^16 cm^3, doping concentration of the source/drain contact regions ND = 10^20 cm^3 and mid-gap metal gate with work-function 4.28 eV. The lateral length of the source and drain contacts were considered small (all most zero) to avoid the influence of the series resistance on the current–voltage characteristics. The impact of high-k materials on the performance of GAA MOSFET with different group III-V gate materials is verified on 3D simulator.

GAA MOSFET with InGaAs shows higher drain conductance (g_d), early voltage and higher drive current. The simulation results prove that use of high-k materials in GAA MOSFETs reduces the Off current and gives better controllability.

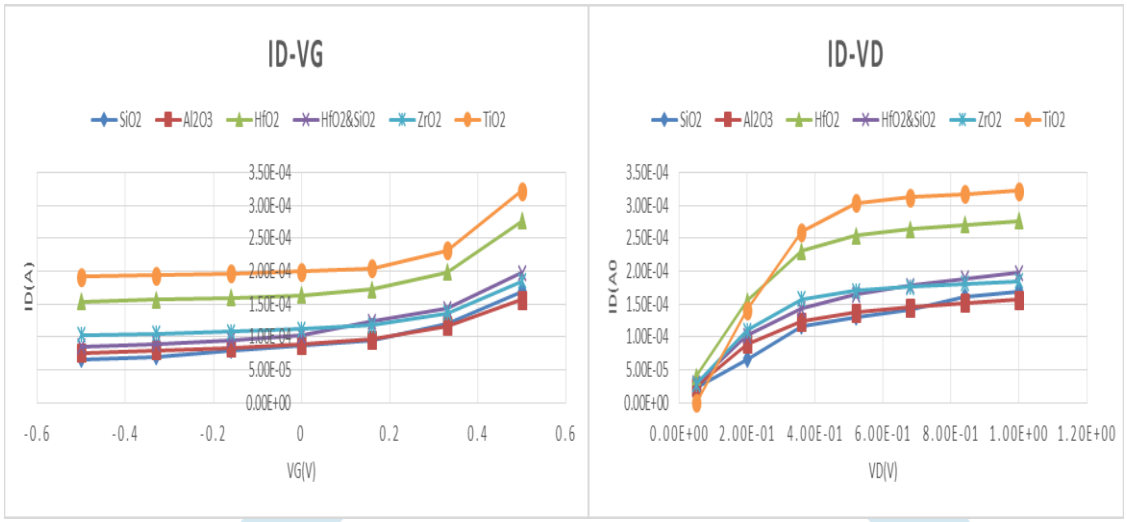

Figure 3: I_d-V_g and I_d-V_d comparison of GAA MOSFET (with InP-gate, V_{gb}=0.5, l=45m, t=2nm, N_d=2*10^20cm^-3, L_{sd}=50nm, t_{ch}=30nm, at v_d=1v and v_g=0.5v)

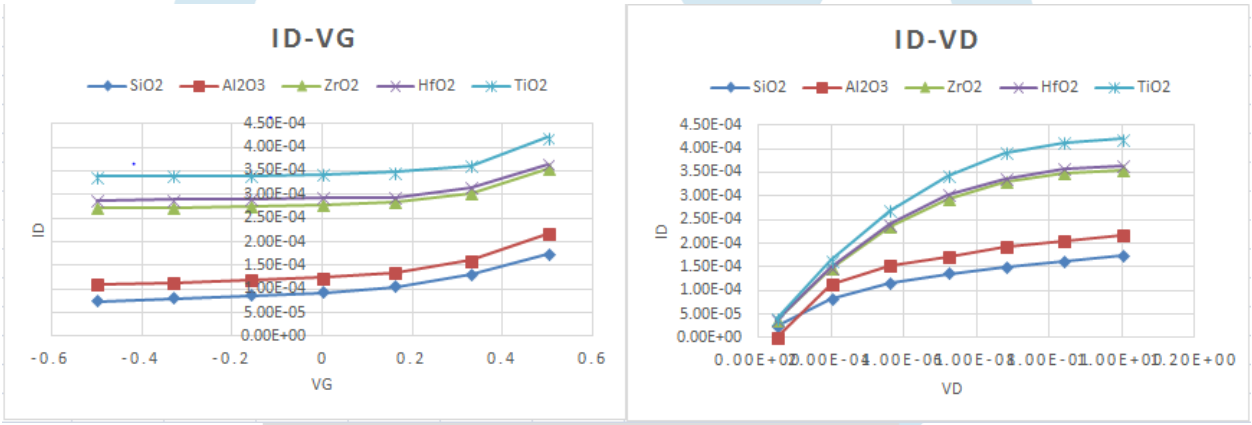

Figure 4: I_d-V_g and I_d-V_d comparison of GAA MOSFET (with InGaAs-gate, V_{gb}=0.5, l=45nm, t=2nm, N_d=2*10^20cm^-3, L_{sd}=50nm, t_{ch}=30nm, V_d=1v and V_g=0.5v)

In FinFETs drain-conductance, g_d, is the change in the drain current divided by the change in the gate to source voltage with a constant drain to source voltage.

$$g_d = \partial Id/\partial Vg$$

The subthreshold swing (SS) of a device is defined as the change in gate voltage which must be applied in order to create a one-decade increase in the output current.

V. Conclusion

Gate All Around FinFET is designed for various group III-V gate dielectrics instead of SiO2 possible high-k materials are InP (k~9), GaAs (k~25), InGaAs (k~80) are used. The device performance is analyzed by replacing the SiO2 with various high-k materials and the characteristics are analyzed. The Gate all Around MOSFET with InGaAs shows improved drain-conductance, early voltage and higher drive current. The simulation results prove that use of high-k materials in Gate all Around MOSFETs reduces the Off current and gives better controllability.

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