CMOS Voltage Controlled Oscillator (VCO) Design with Minimum Transistors

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ABSTRACT:-

This Paper describes the design of complementary Metal Oxide Semiconductor - Voltage Controlled Oscillator (CMOS - VCO). Design which is more and simple area efficient method, since the other methods uses complex architectures of Current Starved VCO'S.

Generally VCO'S uses more number of Transistors that occupies Larger Area and consumed more power. This Current Starved VCO introduces huge amount of parasitic effect, which is undesirable but it is also unavoidable. Their effect can be minimized by using CMOS Based Ring Oscillator VCO. This is because of the usage of less number of transistors in Ring Oscillator VCO. This Paper involves the designing of VCO using Ring Oscillators.

At first, the Inverters are designed. Then, these inverters are replicated to form Ring Oscillator. The Ring Oscillators in this Paper uses Three Stage Inverters. Ring Oscillator VCO consumes less area and less power since they use less number of Transistors compared to Current Starved VCO. Design and Performance Analysis of VCO is done in cadence schematic editor using Cadence Virtuoso 180 nm technology. This approach results in the reduction of Area by minimizing transistors in an operating Frequency of 3.42 GHz with the Power supply of 1.2 Volt. This report includes the results that are obtained during circuit simulation.

Keywords-VCO, CSVCO, Inverter and ring oscillator

1. INTRODUCTION

A Voltage Controlled Oscillator (VCO) is an electronic oscillator in which voltage input controls the oscillation frequency. The Instantaneous Oscillation Frequency is determined by the applied input Voltage. Frequency Modulation or Phase Modulation may be caused by modulating signals which is applied to control input. A part of the Phase Locked Loop and Transceiver consists of Voltage Controlled Oscillator.

Wireless Transceivers and many other electronic systems uses Voltage Controlled Oscillator block widely. The noise performance of the VCO determines the Reception Quality of the signals in any Wireless standard. In Integrated circuits, the parasitic components are undesired but are unavailable.

This parasitic effect may be Overcome when they are taken into account during the initial phase. The Circuit becomes too complex when more number of transistors are used in the design. Hence, the Current Starved Voltage Controlled Oscillators (CSVCO) is not preferable to use. The Current Starved Voltage Controlled Oscillator includes huge amount of parasitic effect since it uses large amount of transistors. Different types of VCO available in which one of them is Ring Oscillator based VCO. Easy Integration is the main reason for the wide popularity of the Ring Oscillator VCO'S.

2. Methodology:

Current Starved VCO architecture consists of two parts: The Inverter Stages and Current starving circuitry. The architecture of this Current Starved VCO is shown in the below Figure 2.1

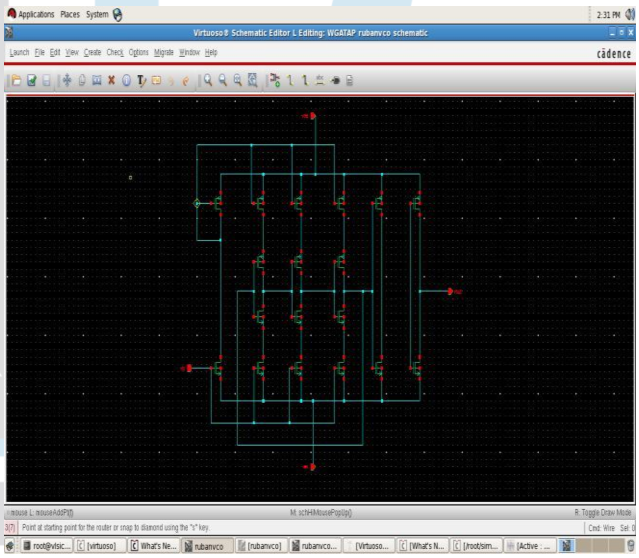

Figure-1 Current Starved VCO Architecture

The problems identified from the above architecture include:

- ✓ Usage of more number of transistors.
- ✓ Increased parasitic effect.
- ✓ The Reception Quality of the signal is very poor.
- ✓ Quality of Service (QOS) is at the lower level due to the complexity in the design.
- ✓ Unable to achieve Frequency stability.

2.1 The Inverter stages

CMOS (Complementary MOS) Inverter is analyzed for the investigation of circuit level degradation. Using CMOS technology complementary transistors can be easily combined. N-Channel and P-Channel can be combined on a single substrate. There are two transistor types which are connected and processed in CMOS Inverter. N type substrate requires P channel MOSFET (Metal Oxide Semiconductor Field Effect Transistor). For processing commonly P type wafers are used. If necessary n-type well implant is added.

High Noise Immunity and Low static power consumption are the important characteristics of CMOS devices. The power is drawn only momentarily since one of the transistors PMOS or NMOS is switching between on and off states. CMOS devices do not produce much heat as other forms of devices do.

2.2 Current starved circuitry

The tuning range of this type of oscillator is relatively low when compared to Ring Oscillators. Since the tuning frequency is relatively low, the output frequency may fall out of the desired range in the presence of process variation. It is difficult to reduce the Vdd voltage on a CMOS Inverter for the purpose of increasing propagation delay. This includes the gate drive where most of delay changes occur due to reduced Vgs. These are the drawbacks that have to be overwhelmed.

3. PROBLEM SOLUTIONS

The problems that are present in the Current starved circuits can be rectified by means of Ring Oscillators. A device that consists of odd number of NOT gates is referred to as Ring Oscillator. The output of these gates oscillates between two voltage levels (between 0 and 1). The immunity to external disturbances is provided by means of the Ring Oscillator. The output of the last Inverter is fed back to the Input. The input is same as the last output. A Ring Oscillator requires power above threshold Voltage to operate. At this voltage, oscillation starts spontaneously. The frequency of oscillation and the current usage can be decreased by decreasing the applied voltage.

3.1 Operation

Ring Oscillator is one of the members of class time delay oscillators. The Ring oscillator uses odd number of Inverters so that gain can be increased greater than 1. Instead of having one delay element, each inverter contributes delay around the ring of Inverters. Hence, the name Ring Oscillator is given. Ring Oscillator schematic is shown in Figure 3.1

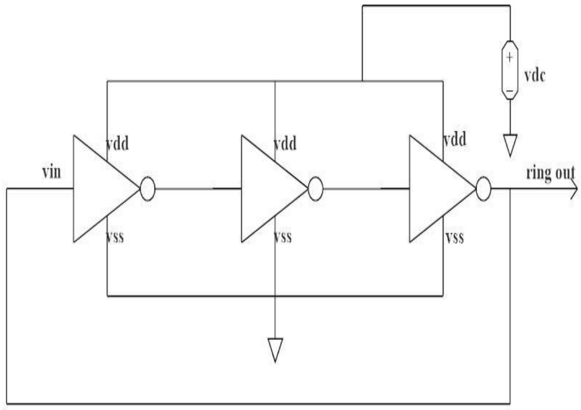

Figure 3.1 Schematic of Ring Oscillator

4. RESULTS AND DISCUSSIONS

In this section, VCO with the Existing Current Starved circuits and the proposed Ring Oscillator VCO are discussed. The Comparisons are made between their advantages and disadvantages in respect of their area.

Table 1 Input Specification

4.1 Voltage Controlled Oscillator

Voltage Controlled Oscillator design first involves the design of precise Inverter with the

Sl. No	Parameters	Values
1	Supply Voltage	1.2 v
2	Technology	Cadence gpdk180 nm
3	Total width	2 um
4	Threshold Value	800 nm
5	Transient time	0 to 200 n
6	Clock Rise Time	1.8 ns
7	Clock Fall Time	1.8 ns
8	Clock Pulse Width	50 ns

Specified values in terms of length, width and threshold values for PMOS and NMOS transistor respectively. Then these compact and specified precise inverter is placed and 3 stage inverters are connected together to form Ring Oscillator VCO. Different parameters and their corresponding values are shown in Table 1. The switching of the device cannot be done quickly shows the existence of gate delay in current starved Inverters. Before current flows through the source and drain, the gate capacitance must be charged. Once the input changes, the output takes a finite amount of time for change to take place. Adding more inverters increases the total gate delay, thereby decreasing the oscillation frequency. But in this Ring Oscillator design only three inverters have been used, thereby decreases the total gate delay, which in turn increases the oscillation frequency.

4.1.1 Design of Inverter

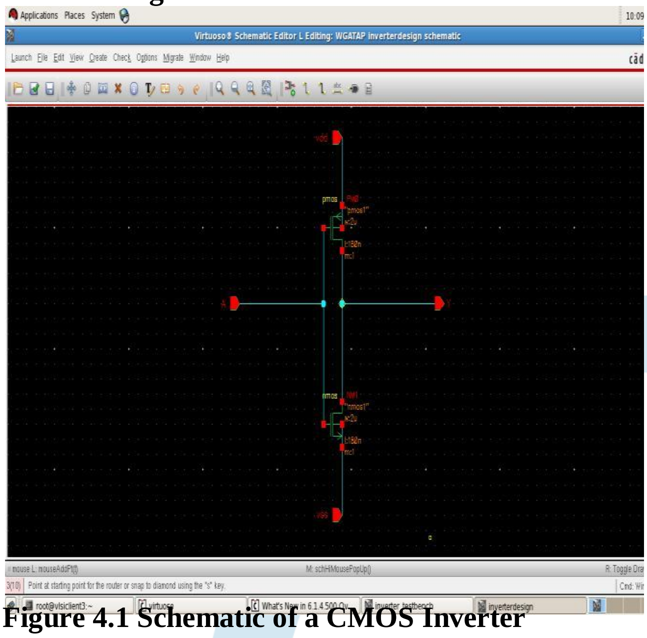

Figure 4.1 Schematic of a CMOS Inverter

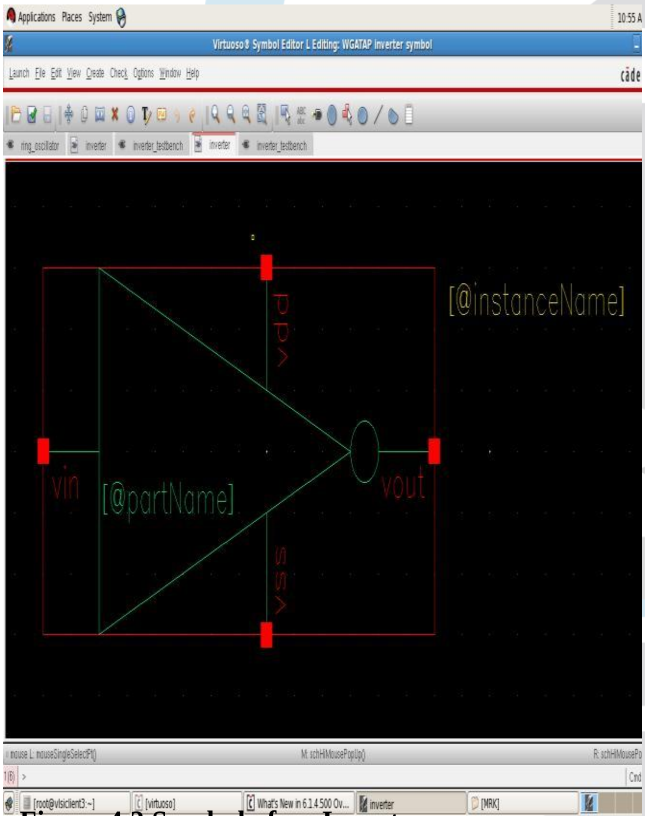

Figure 4.2 Symbol of an Inverter

Figure 4.1 shows the schematic of an CMOS Inverter in which the PMOS transistor and NMOS transistor connected together to form CMOS Inverter. When low input is given, for example (0), PMOS gets ON and high output (1) is obtained. Similarly, when high input (1) is given, NMOS gets ON and low output (0) is obtained. Thus this device can be called as an Inverter, because of its Inverting capability.

4.1.2 Symbol of an Inverter

In Figure 4.2, the symbol of an Inverter is shown. Input pin (Vin) is formed at the left side of the Inverter. Supply Voltage pin (Vdd) is given at the top, Ground pin is provided at the bottom. Output pin (Vout) is at the right side of the Inverter.

4.1.3 Test setup of an Inverter

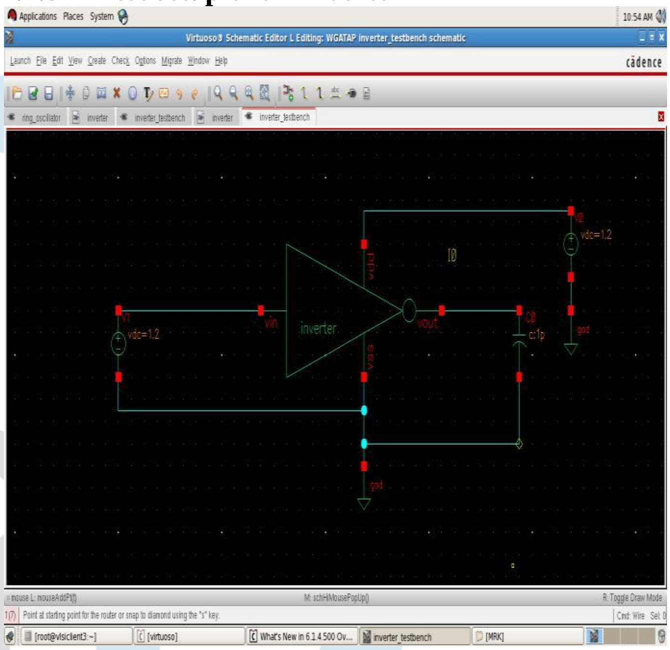

Figure 4.3 Test Setup of an Inverter

Test setup of an Inverter is shown in Figure 4.3. The supply voltage and the input voltage is given as 1.2 volt. The Capacitor C is held at the output for the purpose of storing the charges.

4.1.4 Formation of Ring Oscillator

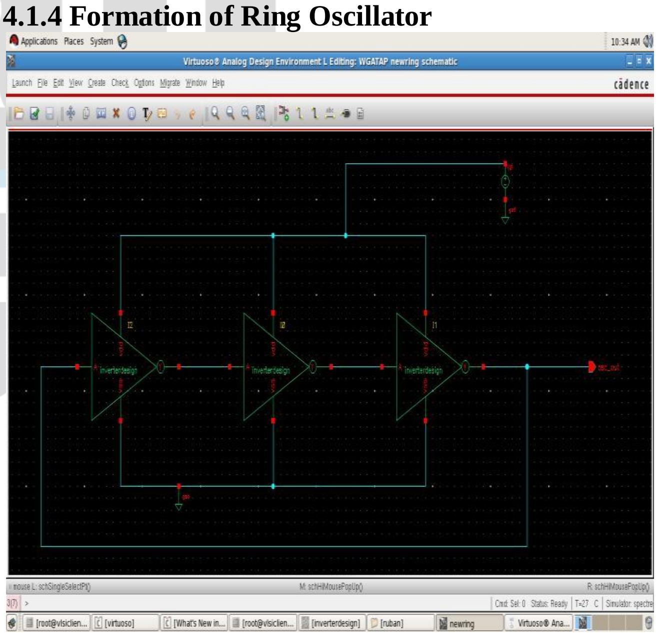

Figure 4.4 Ring Oscillators VCO

The Ring Oscillator shown in Figure 4.4 has three stages Inverter. In this ring oscillator, the output of the first inverter is given to the input of the second inverter and the second inverter output is given as the input of the third inverter. The output of the third Inverter is fed back to the input of the first Inverter, since this is an oscillator. In Figure 4.5, The Transient response of the Ring Oscillator is shown, in which the oscillations are present due to noise in the form of non uniform waveform. The waveform formed has the maximum peak voltage of 1.2 V.

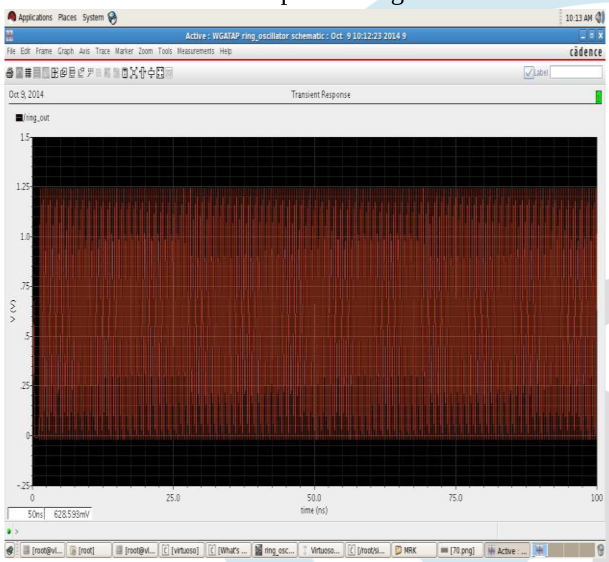

Figure 4.5 Transient response of Ring oscillator

4.2 CURRENT STARVED VCO VS RING OSCILLATOR VCO

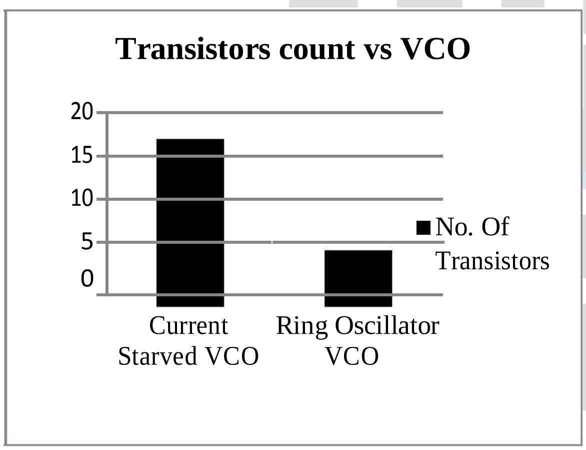

Figure 4.6 Graph representing transistor count between current starved VCO and Ring Oscillator VCO

Better performance is achieved in Ring oscillator VCO by minimizing area. The numbers of Transistors used in Ring Oscillator are three times lesser than the Current Starved Oscillator. Transistor count in Current Starved Oscillator is 18 whereas the transistor count in Ring Oscillator is 6 is shown in figure 5.6.

5. CONCLUSION AND FUTURE WORK

The performance of the VCO Ring Oscillators with the existing oscillators is simulated in Cadence virtuoso analog design environment. GPDK 180nm technology is used with vdd=1.2V as supply voltage. From the simulation results VCO Ring Oscillator with CMOS Inverter have lowest transistor count compared to VCO with current starved Inverter. Thus, the speed of the Modified Ring Oscillator VCO is improved with respect to VCO Architecture with Current Starved Inverters. The comparison results for different VCOs in terms of area are shown in the column graph. From this analysis it is concluded that VCO Receiver with Modified Ring Oscillator is superior to the Current Starved VCO using other Inverters. This Improved VCO can be further implemented along with Phase Locked Loops and Frequency Generators. The modified Ring Oscillator can be further improved by changing the width and length of the PMOS and NMOS Inverter.

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