Design of CNTFET Based Digital Logic and Arithmetic Circuits and ALU

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Abstract---Silicon technology used for high-performance digital circuits and it is a dominant technology for making of integrated circuits. But it continuous to scale down the performance of the digital circuits. So for enhancement of digital circuit performance researchers are further investigating other novel materials to introduce into future technology generations. Carbon Nano tubes (CNTs) have significant advantages for the same due to their excellent carrier mobility. The effect of CNTFET parametric variation for chirality (or diameter) with threshold voltage on performance metrics namely delay and power dissipation in the circuit has been analyzed in the present paper. The I-V characteristics of CNTFET for 1.8 voltsof supply voltage have been performed. A comparative study of CMOS and CNTFET logic circuits is carried out. Various logic gates and arithmetic circuits were designed using CNTFETs; their power consumption and delays are obtained and compared with CMOS. It is analyzed that CNTFET based circuits are energy efficient. The circuits have been simulated using HSPICE for 32nm technology node.

***Index Terms*—CNT; CNTFET; Chirality; HSPICE; I-V characteristics; Threshold Voltage.**

I. INTRODUCTION

The integrated circuit and technology researchers are exploring possible alternatives for the future of the semiconductor industry to enhance the performance of electronic systems. Research is being carried out in evolving high-mobility transistor channel materials such as III–V compound semiconductors, intense the channel material to improve carrier mobility as well as in using non planar transistor structures namely FinFETs and multi gate structures. Simultaneously, novel one-dimensional structures e.g., Nano wires and carbon Nano tubes (CNTs) are also being actively researched. CNTs, with their high carrier mobility, have emerged as a potential candidate to assist the Si technology roadmap in a post 2016 time frame, although numerous challenges remain. Hence, carbon Nano tube field-effect transistors (CNTFETs) provide opportunity for research at both device and circuit levels. This paper briefly describes how carbon nanotube FET improves MOSFET performance. Therefore, CNTFETs need to be extensively studied and used as a possible successor to silicon MOSFETs.

The I-V characteristics of a CNTFET inherit characteristics similar to those of a MOSFET. Using digital logic circuits like Inverter, AND, NAND, OR, NOR and XOR circuits, a comparative study has been carried out for arithmetic circuits (full adder, full subtractor, multiplier) between CMOS and CNTFET technologies in the present work. In order to evaluate the usage of CNTFET technology, parametric variations viz., threshold voltage, diameter of the CNT and supply voltage have been investigated in the present work. Digital circuit design has traditionally been associated with binary logic i.e two logic levels, and this two logic levels are represented by two discrete values of current, voltage or charge. It is established in the literature that carbon nanotubes can be configured to have desired threshold voltages depending on their diameters.

II. CNTFET DEVICE DESCRIPTION

Carbon Nano tubes are ultra-fine unique devices, which can offer substantial advantages over many existing Nano structured materials due to their unusual mechanical, electronic and chemical properties. A typical device structure of MOSFET like carbon nanotube Field Effect Transistor (CNTFET), which consists of drain, gate, source and substrate, is shown in Figure 1.

Carbon nanotube (CNT) made with graphene sheets, which are rolled with certain angle results in carbon nano tube. Depending on the chirality vector (i.e., the direction in which the graphene sheet is rolled), a CNT can be either metallic or semiconducting. This unique property of the Single Walled CNT is referred to as chirality vector and represented by the integer pair (m, n), called the chiral vectors. The nanotube is in metallic nature when n=m or n-m= 3i. Where i is an integer.

In remaining conditions the nanotube is semiconducting. Parallel semiconducting CNTs are grown or transferred to a substrate of CNTFET. The CNT is placed in the channel region and it is kept undoped, but the other two regions are heavily doped, thus forming the source/drain extended region and interconnects between two adjacent devices. The gate voltage then controls the conductivity of these undoped regions. A ballistic or near-ballistic transport can be used to elastic scattering under low voltage bias with CNTs due to the ultra-long (1μm) mean free path (MFP). A typical structure of a MOSFET like CNTFET device is illustrated in Figure 1. By arranging additional CNTs, a linear increase in current can be achieved. Depending on the distance between CNTs (pitch) and the diameter of each CNT, the current cannot be increased linearly with the number of CNTs in a CNTFET because this is due to a small pitch causes the so-called screening effect to occur and the diameter determines the amount of current in a CNT.

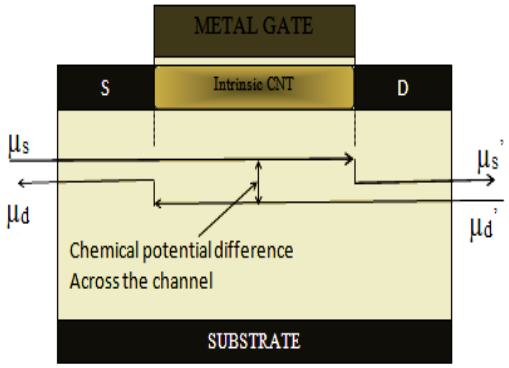

Figure1. 2D device structure of CNTFET.

A carbon nano tube (CNT) is undoped and placed in channel, and the other regions are heavily doped, acting as both source/ drain. For a MOSFET like CNTFET, behavior of both p-type CNTFET and n-type CNTFET are similar. The current density of carbon nano tube (CNT) is very high about 10μA/nm2. Also, CNT has higher carrier mobility compared with MOSFET. In CNTFET ballistic transport mechanism is used. In this mechanism the very same electron that enters one side of the tube appears at the other side of tube shown in Figure 1. It shows the potential difference in channel region with ballistic transport. The conduction of electrons and holes through CNT gives more output current with less threshold voltage.

The energy band gap of CNTFET is inversely proportional to the diameter of CNT (D_{CNT}) is given as

$$D_{CNT} = \frac{a\sqrt{m^2+mn+n^2}}{\pi} \qquad (1)$$

Where, a= 0.249nm is lattice constant, m and n are integers giving the chiral number a vector of CNT. The energy band gap (E_G) in eV of CNT is given as

$$E_G = 0.84/D_{CNT} \qquad (2)$$

For conduction to start, the barrier at source channel junction has to be overcome energy EG/2 (=Δ, say). As barrier height determines the threshold voltage of an FET, the threshold voltage (Vth1) in volts of CNTFET is given as 0.42

$$V_{TH} = 0.42/D_{CNT} \qquad (3)$$

The I-V characteristics of n-type CNTFET are shown in Figure.2. From Figure.2 it can be depicted that the I-V characteristic of n-type CNTFET has same behavior like n-MOSFET. CNTFET simulated by using HSPICE tool with CNT model. CNTFET is a unipolar device like MOSFET. The electrons (NCNFET) or holes (PCNFET) are used for conductivity with heavily doped source/drain. The gate-source biasing modulates the non-tunneling barrier potential in the channel region, and then the conductivity. Better gate electrostatics can be achieved by using high-k, e.g. H_fO, gate dielectric material.

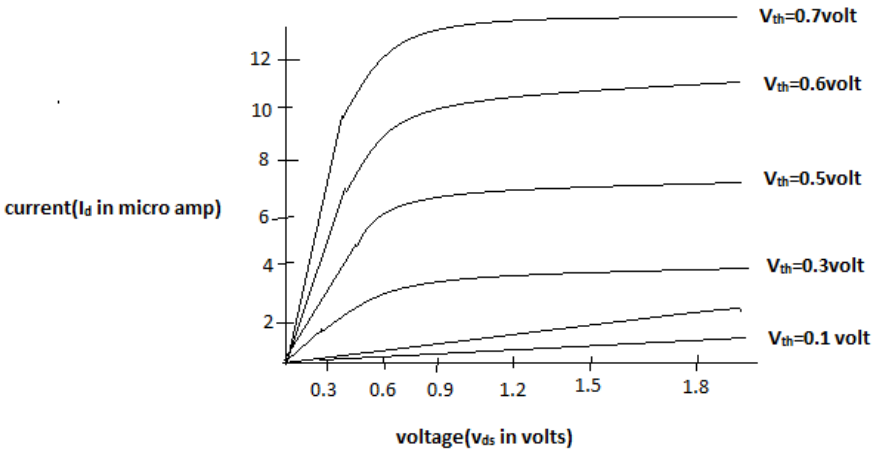

Figure 2. DC characteristics of n-type CNTFET for a supply voltage of 1.8V

The CNT Field Effect Transistor circuit performance changes with the diameter of CNT. By varying chiral vector (m, n) of the tube drain current varies. The variation of threshold voltage with the diameter shown in Figure 2. Supply voltage is 1.8V. It is also seen that with decreasing diameter drain current reduces drastically.

III.SIMULATION RESULTS

This model is designed for unipolar MOSFET like CNTFET devices, where each device may have more than one carbon nanotubes. Hspice 32nm technology with the chiral vector (19, 0) semiconducting with 1.5nm diameter CNT is used. The supply voltage (V_{DD}) given is 1.8V. The variation of gate and drain voltages with supply voltage at V_{DD}.

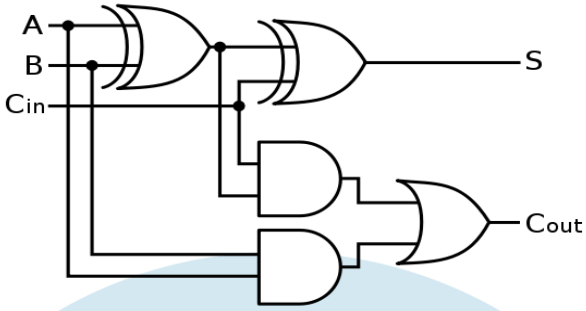

Figure 3. Circuit diagram for full adder

A full adder can be implemented by the composing of basic logic gates. The circuit is showm above. One example implementation is with

Sum= (A Xor B Xor C_{in})
Carry= (A and B) + ($C_{in}$and (A Xor B))

Table 1. Truth table for full adder.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The design of CNTFET based logic circuits and arithmetic circuits has been implemented and simulated by using HSPICE tool.

Figure 4. Simulation Results for full adder

ALU (Arithmetic and Logic Unit):

The circuit is designed for 2-bit ALU. The two input operands are taken as A and B. A0 and B0 are lower significant bits and A1 and B1 are most significant bits. By using we obtain the output depending on the selection lines. X,Y and Z are selection lines. The circuit diagram for ALU as shown in below.

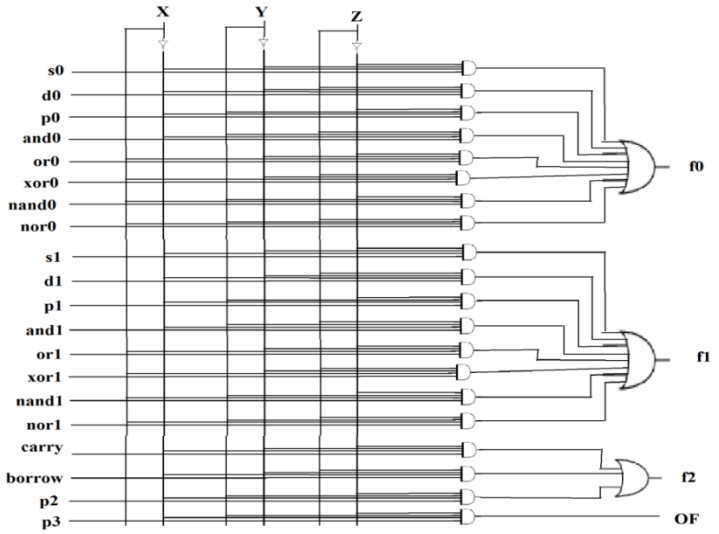

Figure 5 ALU using MUX

In this we can obtain the output. The Selection lines used for ALU operation and their corresponding function for ALU are as shown in table 2.

Table 2 Functional table of ALU

Selection lines			function
x	y	z	
0	0	0	Addition
0	0	1	Subtraction
0	1	0	Multiplication
0	1	1	AND
1	0	0	OR
1	0	1	XOR
1	1	0	NAND
1	1	1	NOR

Figure 6 simulation results for ALU

Full adder, Full subtractor, multiplier and ALU circuits are designed by using CNTFET logic gates. On an average, it is possible to decrease the power consumption and increase the speed of operation with the CNTFET same circuits mapped with conventional MOSFET logic gates.

Table 3.Comparison of power consumption

Circuit	CNTFET	CMOS
Half adder	1.4692E-06	5.5732E-06
Full adder	3.8677E-06	1.3662E-05
Full subtractor	4.5805E-06	1.0607E-05
Multiplier	3.9804E-06	1.5401E-05
ALU	7.1538E-05	2.0962E-04

Table 4.Comparison of delay

Circuit	CNTFET	CMOS
Half adder	2.002ps	19.233ps
Full adder	3.524ps	74.081ps
Full subtractor	3.023ps	73.875ps
Multiplier	2.052ps	75.354ps
ALU	4.985ps	353.6ps

Hspice simulations results demonstrate that the logic and arithmetic circuits achieve great improvement in terms of power delay product with respect to their CMOS counterpart at 32 nm.

IV. CONCLUSION

A comparative analysis of CNT Field Effect Transistor and conventional MOSFET is presented. It is found that the properties of CNTFET match with the properties of MOSFET and so can be very well used as its substitute. Based on the description that the threshold voltage of a CNTFET varies with its diameter, various voltage transfer characteristics (VTC) have been achieved. Basic logic and arithmetic circuit such as all gates, adder, subtractor, multiplier and ALU etc. in CMOS technology and CNTFET technology are implemented and simulated by using HSPICE tool. CNTFET technology provides more efficient way to implement these functions in terms of delay and power consumption. Simulation results show that a reduction in power with low delay can be achieved with CNTFET design. Hence, it is analyzed that CNTFET based circuits are energy efficient.

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