EMC Emissions Reduction Method in Mixed Signal Integrated Circuits with Embedded LIN Driver

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***Abstract*: This paper describes several methods for reduction of electromagnetic emissions (EME) of mixed signal integrated circuits (IC). It is used in an automotive environment, where EMC emission reduction is one of the key success factors. Several proposed methods for EME reduction are described and implemented on three test chips. These methods include current consumption reduction, internal on-chip decoupling, ground separation and different linear voltage regulator topologies. Measurement results of several fabricated test chips are shown and discussed.**

1. Introduction.

The automotive industry is known for a harsh environment for electronic circuits, mainly with respect to used semiconductors, starting with a very wide temperature operating range, ESD pulses, transients present on supply and signal lines, requirements for very low emission and high immunity to electromagnetic disturbances . Due to continuous research in manufacturing technology of integrated circuits (IC), the electromagnetic compatibility (EMC) of electronic systems plays increasing role in circuit performance. The number of devices inside a single integrated circuit and the clock speed increase resulting in higher electromagnetic emissions. Integrated circuits for automotive applications have to be designed with a strong focus on reduction of the EMC emissions. The main focus of the paper is on reduction of EMC emissions of a complex automotive mixed signal IC containing substantial analog content including output drivers, ADCs and DACs, and a digital core including memories and LIN bus drivers. The several methods for electro-magnetic emissions (EME) reduction are discussed and demonstrated on a test chip where the impact of different grounding schemes and supply regulator topologies were tested. Measurement results are presented compared with expectations and conclusions are drawn.

2. EMC Emissions in Integrated Circuits ICs.

2.1 Different Emission Sources

Main on chip EMC emission sources include :

- Clock-driven blocks, synchronized logic
- Memory read/write/refresh
- IO switching
- Switching On/Off heavy load
- Oscillators
- Switching of fast comparators
- Floating domains with high dv/dt transients

The major EMC emission source of the analyzed IC was the digital section. The digital block is the origin of EMC emissions due to the transient current flowing through each elementary logic gate. Supply current peaks occur whenever the logic gate changes its output state either at rising (from logic level "0" to "1") or falling edge(from "1" to "0"), see Fig. 1.1 The combination of several thousands of gates leads to significant current peaks. All on-chip output drivers controlling IC pins are important for EMC emissions as well. Special attention has to be paid to the pins driving wires leaving a module to a cabling harness. High parasitic capacitances and long wires can easily cause significant emissions.

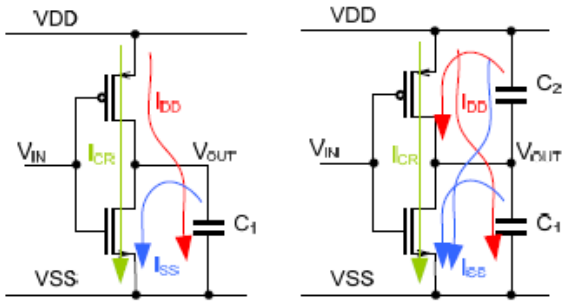

Fig. 1.1, Current path in simple CMOS inverter.

2.2 Coupling Paths.

The emissions generated on a chip can be coupled to the external environment by way of three different principles.

- Conducted emission through the supply lines caused by switching activity of the core and buffers, which induces current drops on the supply pins of the chip.

- Coupling by the IOs: The current spikes provoked by the internal core may be measured on the IOs of the circuit. The PCB wires connected to the IO serve as antennas for the energy.
- On-die radiated coupling: The internal currents inside the chip are responsible for the radiated emissions.

The following chapters are focused on the reduction of conducted emissions in the supply and ground lines and also on the reduction of coupling by IOs. The on-die radiated emissions are not considered in this case since the operating clock frequency of the evaluated chip and its corresponding wave length is negligible considering the die dimensions.

2.3 Emission Reduction.

Examples of good design recommendations include separating signal and power routing, shielding of the sensitive signal tracks, dedicated ground and supply lines for noisy and sensitive blocks EME controlled performance of noisy circuits (i.e. controlled transitions of the power drivers, spreading of the operating frequency) local on-chip/off-chip supply decoupling appropriate package selection , die to package bonding strategy and last, but not least, careful selection of the device layout floor-plan .

2.4 Emission Measurement Methods.

EMC standards used in the automotive industry for evaluation of EMC emissions include CISPR25:2016.The measurement test setup used for the EMC emission performance evaluation compliant with CISP25 withan artificial network (AN) is shown in Fig. 2.1.

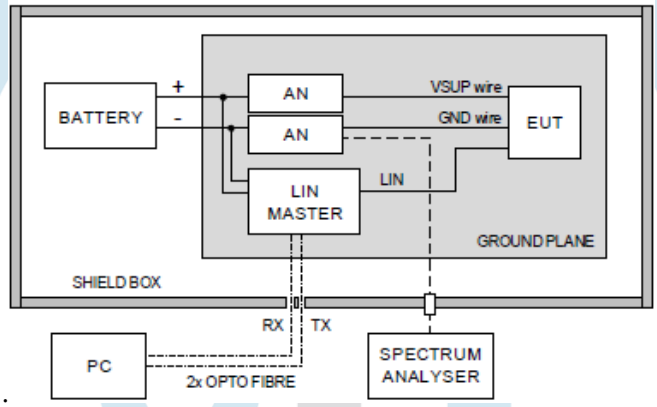

Fig. 2.1 EMC conducted emission measurement setup according to the CISPR25 (AN) with power line remotely grounded.

3. Original Design.

This work was to reduce EMC emissions of a complex mixed signal IC which was not passing EMCemission tests. The original chip was designed in ON Semiconductor high voltage smart power 350 nm technology.

The block diagram of the initial device depicted in Fig. 3.1contains a low-voltage supply (VDD) regulator block which supplies a variety of analog circuitry (like output drivers, measurement channels with ADC, current sources, DAC, etc.), digital circuitry (custom logic, µC, memories) and a LIN block. The module containing this IC is connected to the other modules via a wiring harness with VSUP, LIN and GND wire. The dominant noise source in the IC is the digital block with synchronous logic running at a main clock frequency of approximately 8 MHz. The digital peak current is delivered from the external decoupling capacitor Cext connected between the VDD pin and PCB ground. The peak current flow is depicted in the block diagram in Fig. 3.1. Part of the high frequency current can be delivered from the VSUP pin, depending on the high frequency transfer function of the integrated linear voltage regulator. The VSUP pin is also decoupled by an external capacitor, which will take part of the high frequency current, but the residual part of the current can still flow through the supply line and cause significant EMC emissions, simply because of the length of the current path loop.

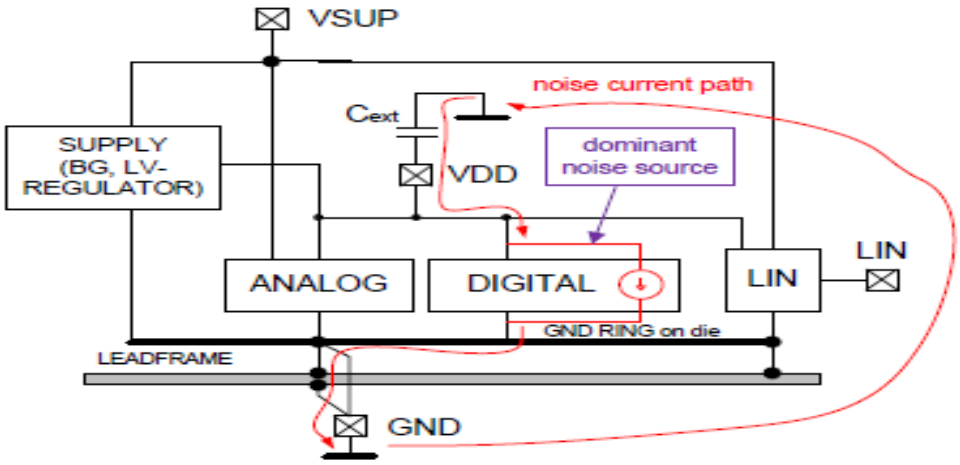

Fig. 3.1. The original device block diagram and noise current path.

Measured EMC emissions on the GND line according to the CISPR25 method are shown in Fig. 3.2. Significant peaks above target limit are visible in the frequency range from 10 MHz up to the 120 MHz. The main peaks are at frequencies 30 MHz and 60 MHz (multiples of the main oscillator frequency).

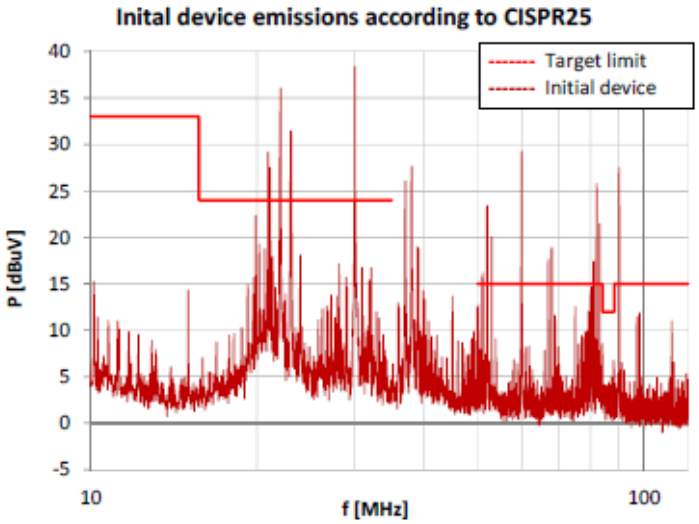

Fig. 3.2. The original device EMC emissions according to the CISPR25, AN method.

4. Reduction of EMC Emissions.

After a detailed study of the EMC emission sources and coupling paths, three different test chips were designed, manufactured and measured for EMC emissions. Different packages were used to split supply and ground connections. In addition, the connection of a lead frame to the PCB ground has been done in a different way. The original device had the lead frame connected to the ground in a single point, primarily to increase the ESD robustness, leading to the shared grounding of the sensitive and noisy blocks. All of the test chips had the lead frame connected at two points in order to eliminate this shared ground path of the noisy and sensitive blocks (required ESD robustness was also reached in this configuration).

4.1 Splitting of Grounds and Local Decoupling.

The following three techniques for EMC emissions reduction were applied in the test chips:

- Reduction of the current consumption of the noise source,
- Peak current decoupling as close as possible to the noise generator to minimize the length of the noisecurrent loop,
- Splitting of the supply and ground lines of the analog blocks, noisy digital block and IOs.

For the current consumption reduction of the complete digital section, each sub block was analyzed with respect to the overall current consumption. The standard digital gate library was changed to be more efficient with respect to a relatively low main clock frequency. The result is a smaller unit transistor size, resulting in much smaller input capacitance of each digital gate and a smaller peak current consumption. Also the current consumption of the embedded memories was checked with respect to the clock speed and access time. total average current consumption of the digital block was The successfully decreased by 1/3 while maintaining the main clock frequency at 8 MHz.

Figure 3.1 shows the peak current decoupling path which is too long and badly designed. The followingactions were done in order to shorten this path. To make the path as short as possible, any free space in the digital section was filled by MOSFET-type capacitors connected between the digital ground and the low-voltage supply (VDD). In addition, all power routing and signal routing channels in the test chips were filled by MOSFET-type capacitors. The internal decoupling is very effective for EMC emission reduction because the intrinsic capacitance is placed very close to the noise sources and the parasitic resistances and capacitances of the connections are minimized. The total accumulated on-chip decoupling capacitance was roughly 5 nF.

Because the internal capacitance between the ground and the low voltage supply was large enough for proper device functionality (under EMC), the external decoupling capacitor on low voltage supply Cext was not needed As a result the peak current path is maintained only locally on the chip. The power routing of the noisy blocks was separated from the sensitive analog blocks and thenoisy LIN block, see Fig. 4.1. The LIN block was connected over the LIN bus to the external environment and acts as an antenna for the EMC emissions. The ground connection of the LIN block was separated from the main ground connection. Ground shifts caused by the digital or IO driver switching were no longer emitted by the LIN bus.

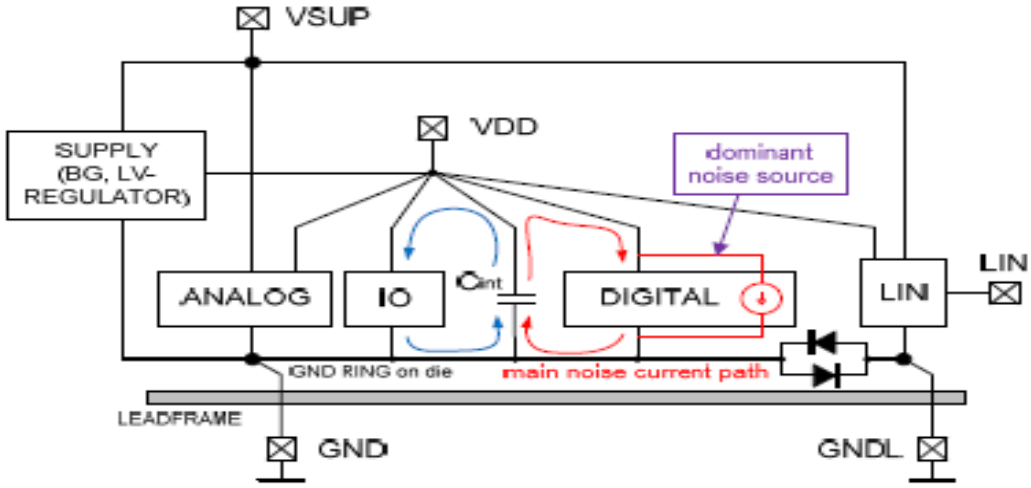

Fig. 4.1. The test chip version 1, block diagram and noise current path.

The EMC emissions of the test chip 1 were measured and compared with the performance of the original device (see Fig. 4.1).The measured emissions of the test chip 1 dropped about 10 to 20 dB and the peaks were able to fit within the target limits. The biggest reduction was seen at the fourth harmonic frequency of the main oscillator around 32 MHz (oscillator of the original device was not calibrated so the main clock frequency was shifted to 7.5 MHz).

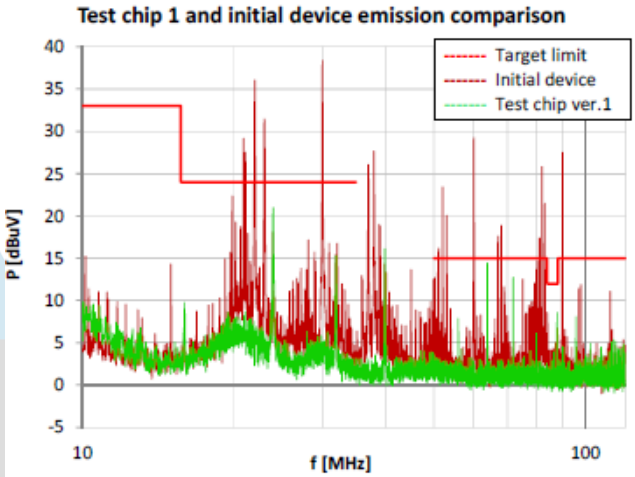

Fig. 4.2. EMC emission comparison of test chip with the original device, CISPR25, AN method.

4.2 Splitting of Ground Pins.

The original device and the test chip 1 were assembled in the SOIC16 package. Due to its limited pin count, the number of pins dedicated to ground and supply connections were limited. To overcome this limitation a QFN 32 package was used and the ground and supply connections were extended in the test chip 2 (see Fig. 4.3). The ground lines were split. For instance, the IO drivers have separate ground connections and some ground pins and the bond wires were placed in parallel in order to decrease the impedance of the connection to the PCB and, consequently, the voltage drop. The EMC emission performance comparison between the two package types is shown in Fig. 4.4. The measurement results of test chips with different packages show that the emissions can be further decreased at some frequencies by 3 to 10 dB simply by a proper separation of the ground and supply lines.

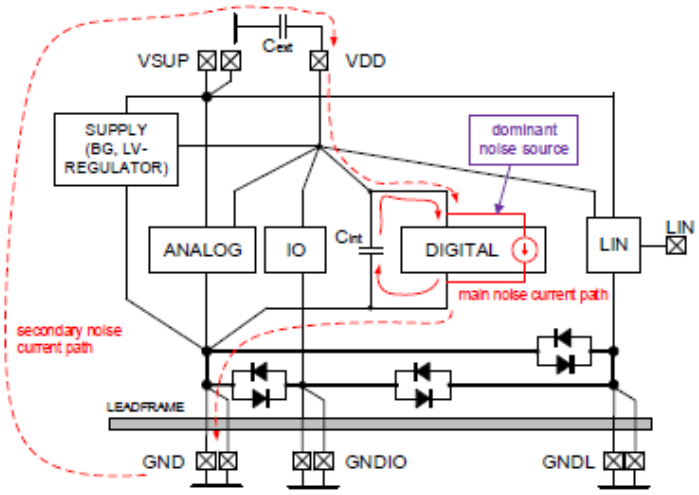

Fig. 4.3. Block diagram and noise current paths of test chip #2 and #3.

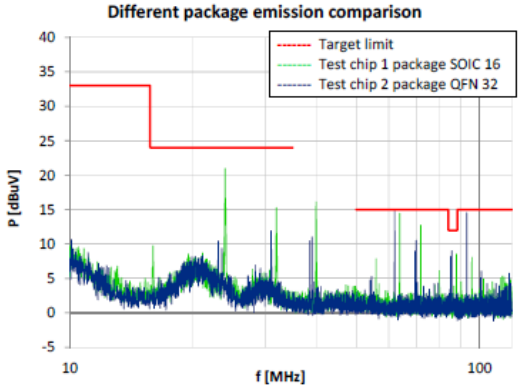

Fig. 4.4. EMC emission comparison of test chip in different package options, CISPR25, AN method.

4.3 Linear Voltage Regulator Topologies.

The impact of the linear voltage regulator topology on EMC emissions was tested using two types of regulators. The original device and test chip 1 and 2 were manufactured with source follower linear voltage regulators with an NMOS-type output transistor (Fig. 4.5). The dominant pole resides inside the regulator block so there is no need of an external stabilization capacitor. The decoupling capacitor for ripple reduction can be kept internally, on chip. Test chip 3 was equipped with an LDO type regulator with a PMOS-type output transistor, which was stabilized by a dominant pole on an external decoupling capacitor. All internal poles in the regulator were well above the gain bandwidth of the regulator. An external stabilization capacitor CEXT of 1 µF was connected between VDD and GND pins. An EMC comparison of the regulators comprised of PMOS and NMOS-type output stages has been further discussed in. The voltage regulator with a PMOS output stage has been found superior compared to the regulator with an NMOS output stage. Results of the comparative measurement of the conducted EMC emissions are shown in Fig. 4.6. Test chips in QFN32 packages were measured.

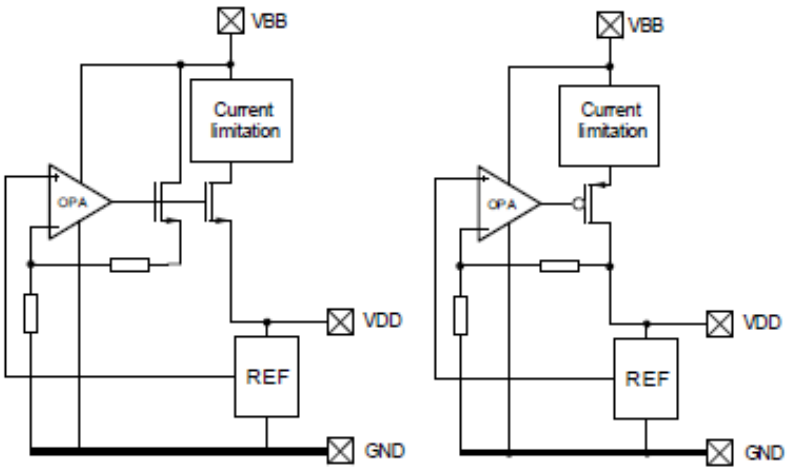

Fig. 4.5. Linear voltage regulator topologies, source follower (left) and LDO (right).

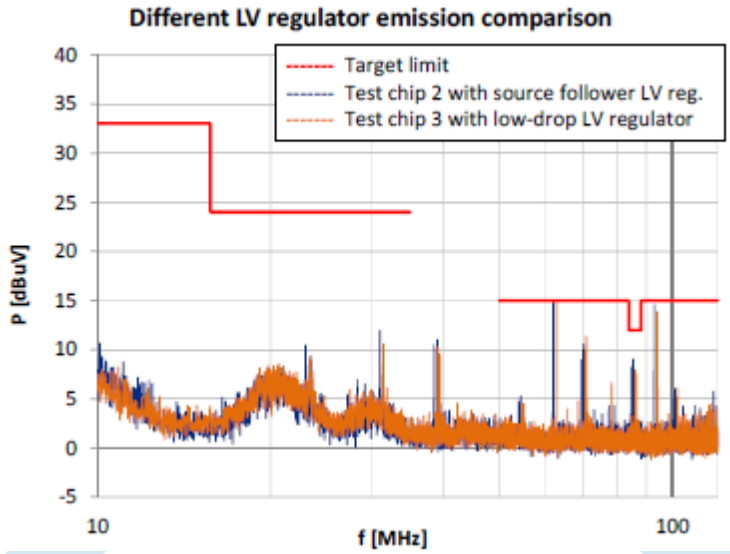

Fig. 4.6.EMC emission comparison of different low voltage regulator structures used in test chips.

No significant difference in EMC emissions between the two regulator topologies was observed. This could be the result of the effectiveness of all previously disclosed methods for EMC emission reduction where a minimum of emissions is coupled through the regulators and the remaining coupling paths are outside of the regulators.

5. Conclusions.

This paper focuses on practical EMC emissions improvements to a complex mixed signal IC for automotive applications with an embedded LIN driver in the frequency range from 10 MHz to 120 MHz. Several techniques were discussed and implemented in the test chips and measured. Measurement results were compared with the initial device. Significant improvements of about 10 to 20 dB were achieved by current consumption reduction, internal on chip decoupling and separation of the LIN block ground. Further reduction of the EMC emissions in a lower frequency range was reached with the QFN32 package where more pins were available and the supply and ground pins were further split. Finally, the two different topologies of linear voltage regulators were compared and no significant difference in EMC performance of the complete test chips was observed.

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