Reversible BCD Adder Emphatic Design and Exertion

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***Abstract*:- In the past few decades Reversible logic is one of the most significant research area Reversible logic allows low power dissipating circuit design and founds its application in quantum computing, digital signal processing, cryptography and optical information processing.BCD adder is an essential component for processors and optimized design of these adders. In this paper an augmentation method is proposed to realize a reversible Binary Coded Decimal adder using HNG, Fredkin, and Feynman and Peres gates. It had been evidence that the suggested design offers less hardware involvement. This recommended reversible BCD adder is evaluated and optimized in terms of quantum cost and gate count, result in high speed BCD adder with optimized area.**

***Keywords*: Emphatic design, Garbage Output, Reversible Logic, Quantum Cost, Binary Coded Decimal Adder.**

I. INTRODUCTION

Reversible logic has wide applications in the area of quantum computing, optical information processing, digital signal processing and nanotechnology. Power dissipation more and more becomes a critical issue for designing high performance digital circuits. Landauer proved that combinational logic circuits dissipate heat in an order of kT log 2 joules for each "lost" bit information during the irreversible operation, where Boltzmann constant k=1.3807 x 10 -23 joule s per kelvin and T is the absolute temperature. Bennett showed that energy dissipation is reduced or even eliminated if a computation were carried out in a reversible way. Reversible Gates are circuits in which number of inputs is equal to the number of outputs and there is a one to one mapping between the vector of inputs and outputs. Its not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. For reversible logic, the data is bijectively transformed without losing any of the original information. The following constraints is to be considered in the design synthesis of reversible gates

- The number of outputs of a reversible logic must be equal to the total number of inputs.
- The output of the reversible gate is not used as a primary output or as input to other gate is called garbage outputs.
- The number of constant inputs to the gate should be as minimum as possible.
- In reversible logic, fan-out is not allowed; every output can be used once at a time.
- In reversible logic, quantum cost should be minimum as possible.

Reversible computing is one of the solution for reducing power dissipation which is alternative for conventional logic. Reversible computing will fundamentally affect the speed of circuts.

II. LITERATURE SURVEY

Design of reversible BCD adders have been proposed in [1] with a goal of optimizing number of ancilla bits and garbage outputs. In the paper [14] proposes synthesis method to realize a reversible BCD adder circuit, where delay is not taken into account. In the paper [9] BCD adder has been designed using New gates and FG gates, where they considered only garbage outputs and quantum cost, delay and ancilla inputs have not been discussed. In this work, a new over 9 detection circuit scheme is proposed and used 4-bit parallel adder with HNG gate design [8] unlike MKG and TSG gates. So that overall quantum cost of the circuit is reduced and it is compared with previous works. Because of reduced quantum cost, delay and gate count which makes it more efficient in terms of area and delay. Basics related reversible logic gates are discussed in section III. Block diagram of BCD adder is discussed in section IV. Proposed method is discussed in section V. Experimental results are presented in section VI. Concluding remarks are discussed in section VII.

III. BASIC REVERSIBLE LOGIC GATES

To realize any reversible logic some constraints must be follow: fan outs and feedback are not directly allowed. Since they collapse the reversibility of the computation. The traditional design flow is not used. So that, a cascade

structure over reversible gates is established while we realizing a reversible logic model.

A. Feynman

Feynman gate is a 2*2 reversible logic gate as shown in Fig.1. It is also called as one through reversible gate. The input vector is (A, B) and the output vector is (P, Q). The outputs are defined as P=A, Q=A ⊕B. Quantum cost of a Feynman gate is one. Feynman Gate (FG) acts as a copying gate. Since a fan-out is not allowed in reversible logic, so that this gate is useful for replica of the required outputs.

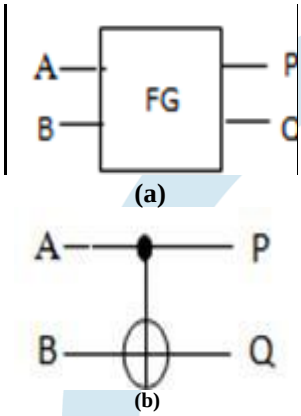

Fig.1. (a) FeynmanGate (b) Quantum symbol.

TABLE I: Truth Table Of Feynman Gate

A	B	P	Q
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

B. Fredkin

Fredkin gate shown in fig.2, is a 3*3 reversible gate. The input vector is (A, B, C) and the output vector is (P, Q, R). The output is defined by P=A, Q=$\bar{A}$B ⊕ AC and R=$\bar{A}$C ⊕ AB. Fredkin gate is a universal gate, so that we can construct the basic gates such as AND, OR, NOT and other gates from this Fredkin gate by presetting some of its inputs.Quantum cost of a Fredkin gate is 5.

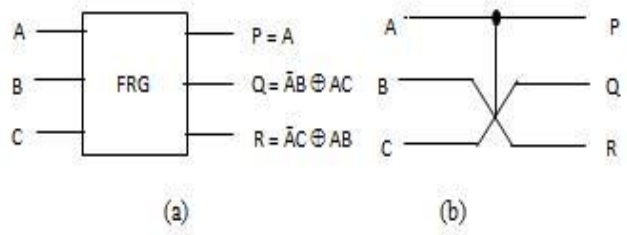

Fig.2. (a) Fredkin gate (b) Quantum symbol.

TABLE II: Truth Table Of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

C. Peres Gate

Peres gate is as shown in fig.3, is a 3*3 reversible gate. The input vector is (A, B, C) and the output vector is (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R=AB ⊕ C. Quantum cost of a Peres gate is 4. In the proposed scheme, Peres gate is used for its lowest quantum cost.

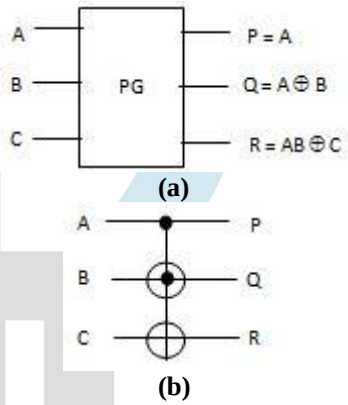

Fig.3. (a) Peres gate (b) quantum symbol.

TABLE III: Truth Table Of Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	0	0

D. HNG Gate

HNG gate is as shown in fig.4, which is a 4*4 reversible gate. The most significant aspect of the gate is, it can work individually as a reversible full adder The input vector is (A,B,C,D) and the output vector is (P,Q,R,S). The output is defined by P=A, Q=B, R= A⊕B⊕C and S= (A⊕B)C⊕AB⊕D. Quantum cost of a HNG gate is 6.

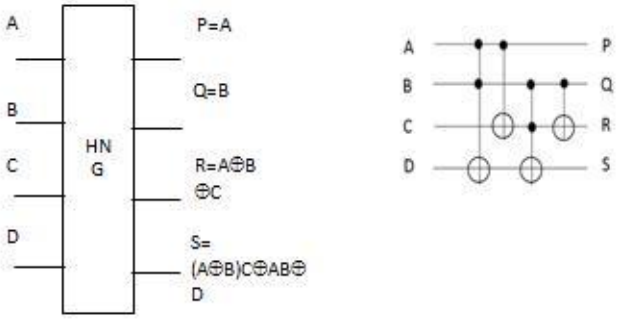

Fig. 4. (a)HNG gate(b) Quantum symbol.

TABLE IV: Truth Table of HNG Gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	1
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Where, Quantum cost denotesthe cost of the circuit in terms of cost of a primitive gate. It is calculated by knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Always it should be minimum as possible.

IV. BLOCK DIAGRAM OF BCD ADDER

BCD adder circuit adds two BCD numbers and the result also is in BCD form. The block diagram of BCD adder is as shown in Fig.5. In the block diagram of BCD adder, there are three major parts – binary adder, detection circuit and correction unit.

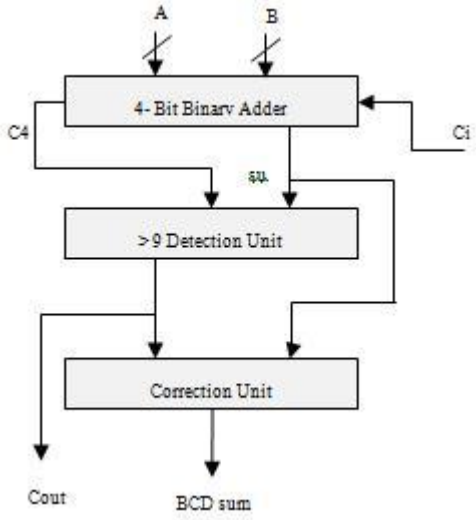

Fig.5. Block Diagram of BCD Adder.

Binary adder performs addition of two BCD numbers and a carry bit as input. Detection circuit is used to detect the result of binary adder is greater than 9 or not. If the result is greater than 9, then it produces „1" otherwise „0".correction unit, if the detection circuit output is „1" then the 1st 4-bit adder sum is added by $(0110)_2$ otherwise $(0000)_2$.

V. PROPOSED DESIGN

A. Four Bit Reversible Parallel Adder

In this work, BCD adder is going to implement using eversible logic gates. The first part, 4-bit parallel adder using HNG reversible logic gates is as shown in Fig.6 which can also be constructed using TSG or MKG gates.

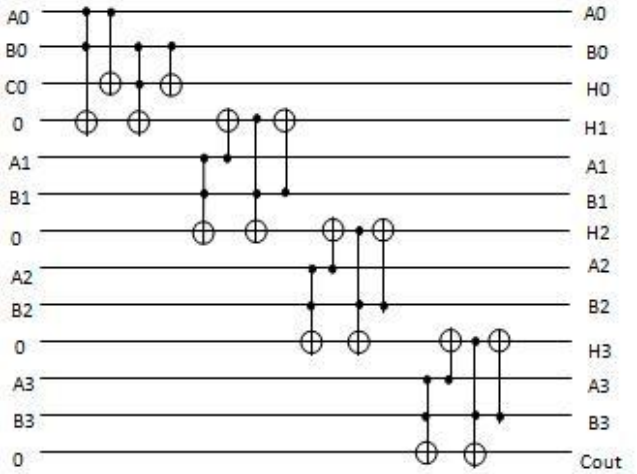

Fig.6. reversible 4-bit parallel adder using HNG gates.

In the reversible 4 bit parallel adder, here 4 HNG reversible logic gates are used. Each HNG gate accepts A, B are two inputs and input carry C0, which produces sum, carry and two garbage outputs.HNG gates having low quantum cost compared to MKG, TSG and DOUBLE PERES gates. So in this paper, we are using HNG gates in

the design of reversible BCD adder. The quantum cost of reversible 4-bit parallel adder is 24.

B. Over 9 Detection Circuit

In the design of reversible detection logic circuit, Peres and Fredkin gates are used. The over 9 detection circuit using reversible logic gates is as shown in Fig.7.

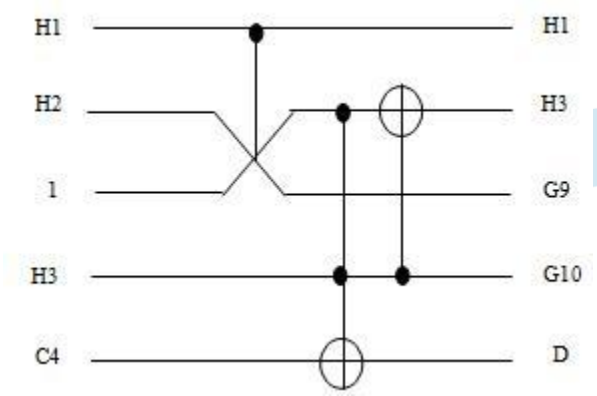

Fig.7. proposed over 9 detection circuit.

Using Fredkin gate, we get (H_1+H_2). Then it is connected to Peres gate. Then the detection logic circuit output is (H_1+H_2) $H_3 \oplus C_4$.Thequantum cost of detection circuit is 9.

C. Design of Reversible 4-bit BCD Adder

In the proposed design of reversible BCD adder, used a 4-bit parallel adder using HNG reversible gates and used a proposed detection logic circuit. One extra Feynman gate is used as copying gate. If the value is greater than 9 then the correction adds 6 to the result of reversible 4-bit parallel adder. In the correction circuit, one Peres, one HNG and one Feynman gate is as shown in Fig.8.

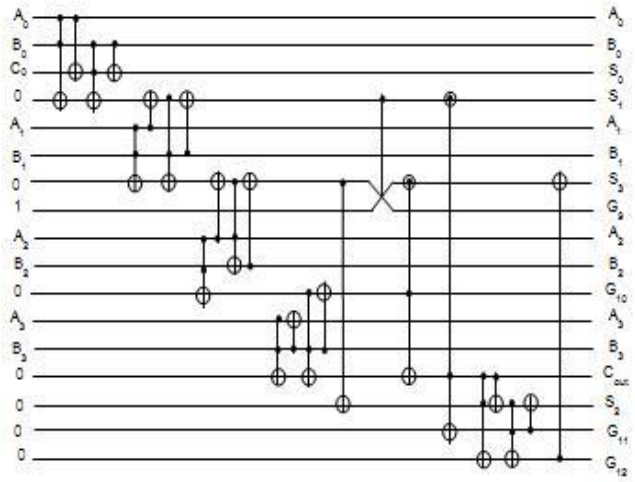

Fig.8. Proposed reversible BCD adder circuit design.

The proposed circuit uses a total number of 10 reversible gates consisting of five HNG gates, two Peres gate, two Feynman gate and one Fredkin gate. The number of garbage outputs in the proposed design is 12. The total delay of the reversible BCD circuit is calculated.

For HNG gate the propagation delay is 6Δ. To the circuit of reversible 4-bit parallel adder, the propagation dealy is 24 Δ. Since 4 HNG gates are cascaded. For detection circuit, the propagation delay is 9Δ. Since the individual propagation delays of Fredkin and Peres gates are 5Δ and 4Δ. Similarly, the propagation delay for correction circuit is 11Δ. Since it is cascaded the Feynman, HNG and Peres gates. The propagation delay for Feynman gate is 1Δ. For copying purpose, 1 more Feynman gate is used. So the total propagation delay of reversible BCD adder circuit is 45Δ. Because of the reduced quantum cost and delay, the complete cost of the proposed circuit is reduced and also increases the performance of the circuit.

VI. RESULTS AND DISCUSSION

The gates are used in the reversible BCD adder are designed using VHDL (VHSIC HDL) language and simulated in XILINX 14.7 ISE. The results using Xilinx simulator are same as the results in circuits. The simulation results are the base of the validation of the circuit designs. The RTL schematic for reversible BCD adder circuit design is as shown in Fig. 9 and the simulated output is as shown in Fig.10.

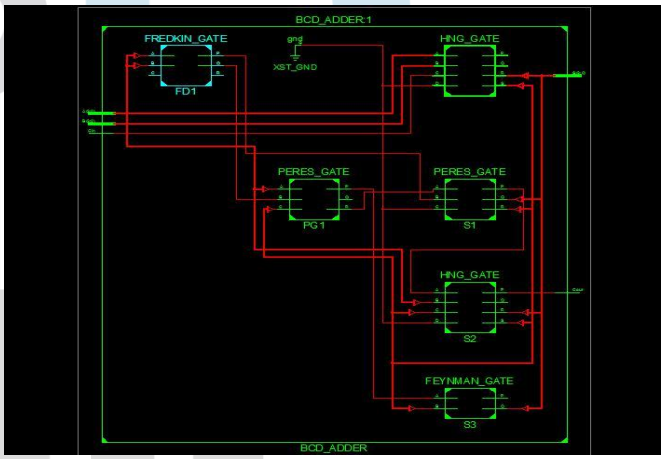

Figure 9. RTL schematic diagram of reversible BCD adder.

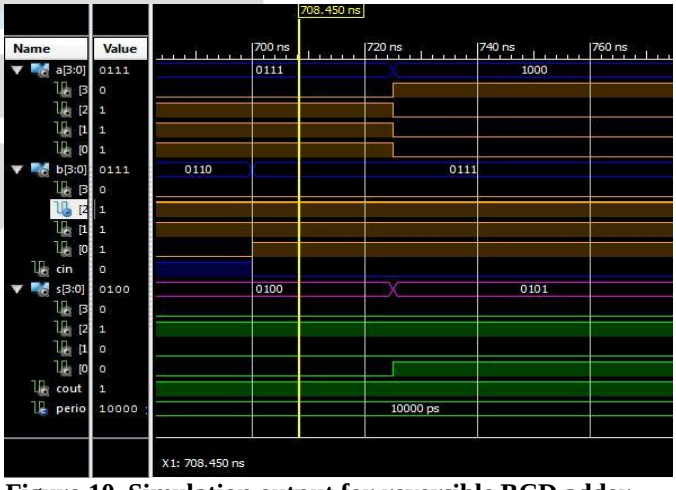

Figure 10. Simulation output for reversible BCD adder.

TABLE I: A Comparison of Reversible BCD Adders

BCD Adder	Gate Count	Quantum cost	garbage outputs	constant inputs	Delay Δ
[8]	14	83	22	17	NM
[9]	23	NM	22	17	NM
[10]	10	55	11	7	NM
[11] (Design 2)	NM	90	6	10	80
Proposed Design	10	45	12	7	45

NM- not mentioned

The proposed reversible BCD adder design, QC (quantum cost) and delay is reduced when compared to previous works as shown in TABLE I.

VII. CONCLUSION

In this work, reversible logic was implemented for BCD adder. By comparing the existing BCD adder design with proposed reversible BCD adder design is less costly in terms of number of gates, quantum cost and delay. Because of these optimization parameters the complete cost of the circuit will be reduced. The design method provide a base to build more computational structures like ALU of a primitive quantum CPU. Alternate design methods are under investigation as a future work.

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