Mitigation of DC Ripples & Reduction in Electrolytic Capacitors by Novel Ripple Elimination Circuit

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***Abstract*: with the advent of power electronic controls in the DC systems, the use of DC power is gaining more importance. But there arises the problem of power quality issues by the ripples generated in the DC system. In the present scenario, the end use devices require high quality, sensible power otherwise would result in the serious malfunction of the devices. This paper presents the control strategies for elimination of ripples and reduction of electrolytic capacitors by pulse width modulation based rectifying approach and continuous conduction mode. The implementation is carried out in Mat Lab Simulink platform. Finally the circuit along with the results to justify the feasibility of ripple elimination & reduction in electrolytic capacitors are been presented.**

***Keywords*: DC ripples, Continuous Conduction Mode, PWM control.**

1. INTRODUCTION

In the present energy scenario, due to the increase in the energy demand renewable energy harvesting is gaining much importance such as wind, solar, tidal etc. in which wind and solar are very promising and predominant. The electricity generated will be in the DC form and is then converted to AC by using suitable converting circuits. These converting circuits are basically power electronic based which introduces harmonics into the system. One such harmonics in DC system is ripples. Ripples are generated during the conversion and affect the operation of the system. Typically the current and voltage harmonics should be less than 10% in order to operate the system normally. Hence there is much necessity to control and eliminate these ripples in the DC system. The simplest way of eliminating DC ripples is to connect a capacitor bank in parallel with the output of the converter circuit. But these large electrolytic capacitors are costly, bulky and more over require continuous maintenance which results in the extra cost and time. The life time of the electrolytic capacitors are is also less. Hence in order to optimize the performance a novel DC compensation circuit is developed which would eliminate the ripples & improve the quality of supply. The DC compensation circuit is basically a controlled buck- boost circuit whose output depends on the controller error signal which will try to maintain the constant DC voltage across the load. Various control strategies are presented to improve the system performance by elimination of ripples.

2. BLOCK DIAGRAM

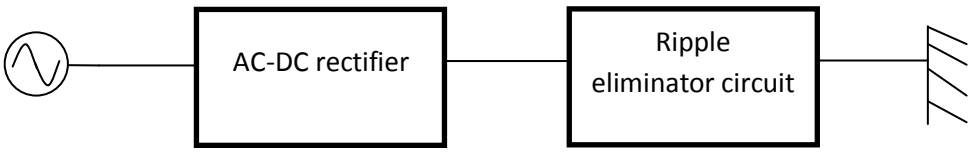

Fig 1: single line diagram of proposed system

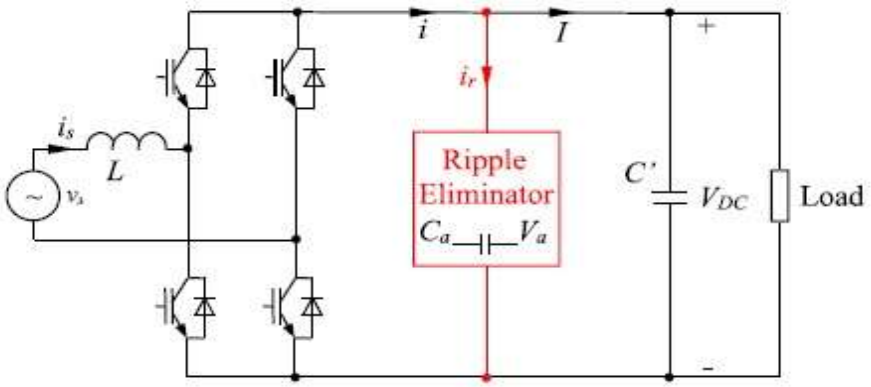

Fig 2: proposed control model

Figure shows the single line diagram and block diagram of the proposed model scheme of control. Single phase AC supply is considered which will be rectified to generate the DC, during which ripples are generated. A ripple eliminator circuit is connected in shunt as shown which are made of IGBT's. The output of the ripple eliminator is connected to the load.

3. PROPOSED METHDOLOGY

The proposed methodology is to make an alternate way to pass the ripple power such as connecting the energy source in parallel with the circuit. Figure 3 shows the topology of the ripple eliminator circuit. Basically this is an buck and boost circuit along with the energy storage devices as capacitor and inductor, where these energy storing devices act as parallel path for ripple power flowing. The voltage ripples are eliminated by keeping the load current at a constant value which is accomplished by the inductors as shown, and similarly in order to eliminate the current ripples the capacitor must discharge whose time is very important. Hence the continuous conduction mode is chosen for charging and discharging sequence of the capacitor. The energy stored in capacitor can be given as,

$$E = \frac{1}{2}CV^2$$

And the ripple energy as,

$$\frac{1}{2}C_a\left(V_{a0}+\frac{1}{2}\Delta V_a\right)^2-\frac{1}{2}C_a\left(V_{a0}-\frac{1}{2}\Delta V_a\right)^2=C_aV_{a0}\Delta V_a$$

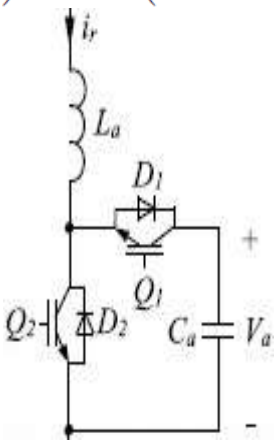

Fig 3: ripple eliminator circuit

From the above equation it is clear that the voltage and capacitance are inversely proportional to each other. Hence for higher value of voltage the capacitance value decreases, which can be stated as reduction in the electrolytic capacitors. In the charging mode the circuit behaves as the buck converter and in the discharging mode it behaves as the boost converter. The two modes are given in detail

A) During Charging Mode

In this mode the current (i_r) is positive and the ripple eliminator circuit transfers all the ripple power to the capacitor (C_a) through the inductor (L_a).Here Q2 is OFF and Q1 takes the signals from PWM circuit.
When Q1 is ON the duty cycle can be given as $D=T_1/T_r$. and the inductor current increases to take up the DC voltage (V_{dc}).
When Q1 is OFF the inductor current decreases till the capacitor (auxiliary) value is reached.

B) During Discharging Mode

In this mode the current (i_r) is negative and the energy storage discharges the stored energy into the circuit through the capacitor. Here Q1 is always OFF and Q2 takes the signals from the PWM circuit.
When Q2 is ON the duty cycle can be given as $D=T_1/T_r$, the inductor takes up the auxiliary circuit current value.
When Q2 is OFF the inductor current feeds the DC bus voltage, whose waveforms are as below

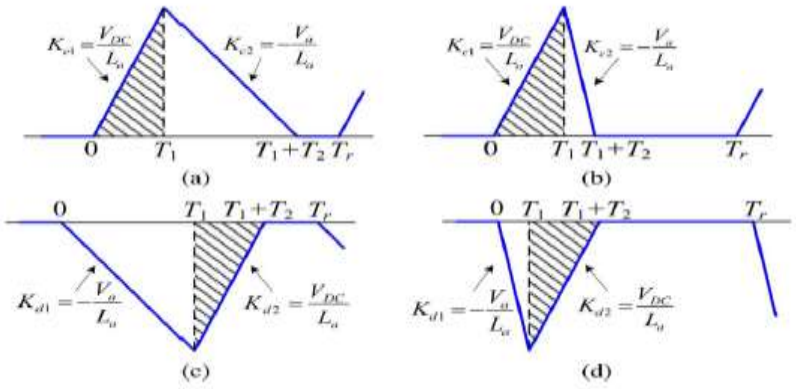

Fig 4: waveforms of operation

4. SIMULATION& ANALYSIS

The circuit is simulated in the Mal Lab Simulink software in order to justify the proposed modelwhich is shown in figure 5. For the PWM and Capacitor, the pulse generation circuit is as in fig 6. The block parameters are taken from the reference paper [1]. And the simulation is carried out in two cases with ripple eliminator and without ripple eliminator.

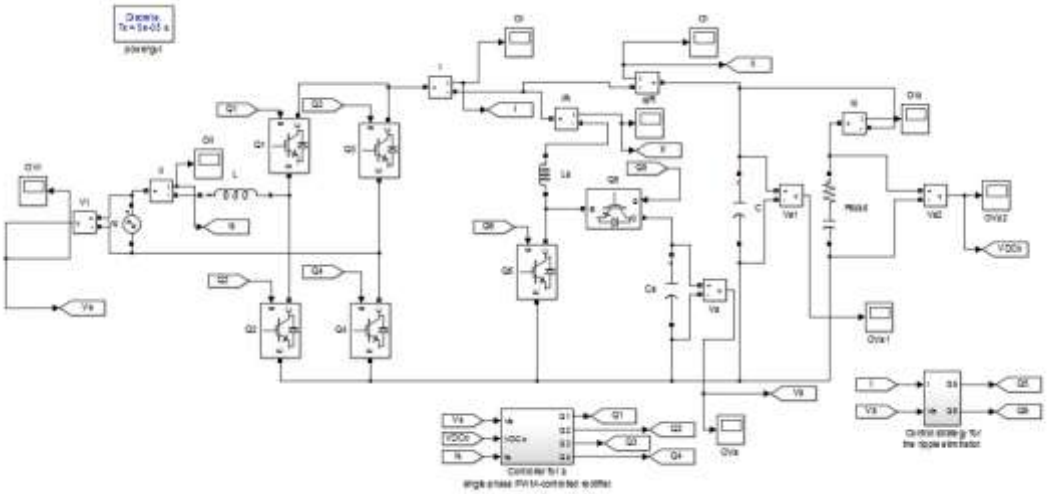

Fig 5: overall simulation model

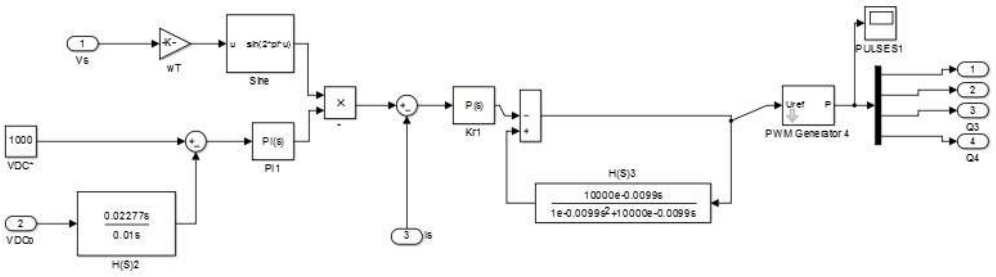

Fig 6: pulse generating circuit

The output of the dc system when ripple eliminator is not connected contains ripples which is as shown here,

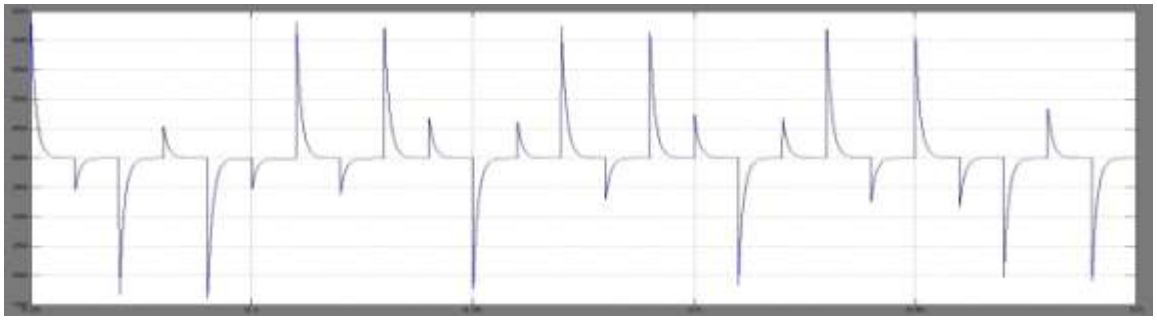

Fig 7: without ripple eliminator output

And the output of the circuit when ripple eliminator is connected can be given as,

Fig 8: output across DC bus with ripple eliminator

5. CONCLUSION& FUTURE SCOPE

From the above discussion and the simulation and waveform studies we can conclude that this PWM based approach holds very well to eliminate the ripples as well as to reduce the electrolytic capacitors. Hence the power quality of the DC bus is increased. The future scope lies in the implementation of the control scheme into the hardware module and to test the hardware for practical feasibility.

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