Mitigation of Flicker Sources & Power Quality Improvement by Using Cascaded Multi-Level Converter Based DSTATCOM

[1]Siddartha A P, [2]B Kantharaj, [3]Poshitha B

[1]PG Scholar, [2]Associate Professor, [3]Assistant Professor
Department of EEE, VTU
Adichunchanagiri Institute of Technology, Chikkamagalur, india

***Abstract*— Modern power systems are of complex networks where hundreds of generating stations and thousands of load centres are interconnected through long power transmission and distribution networks. Even though the power generation is fairly reliable the quality of power is not always so reliable. Power system especially distribution systems have numerous nonlinear loads which significantly affect the quality of power. Shunt compensation for medium voltage distribution systems require higher rating for voltage source converters (VSCs). Ratings of the semiconductor devices in a VSCarealways limited. Therefore for higher rated converters it is desirable to distribute the stress among the number of devices using multilevel topology. This paper presents an investigation of five-Level Cascaded H– bridge(CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System(PS) for compensation of reactive power and harmonics.**

***Index term*— Power Quality, VSC, DSTATCOM, Reactive Power**

I. INTRODUCTION

Power quality disturbance is generally defined as any change in power (voltage, current or frequency) that interferes with the normal operation of electrical equipment. The study of power quality and ways to control it is a concern for electric utilities, large industrial companies, businesses and even home users. Thestudyhasintensifiedasequipmenthasbecomeincreasingly sensitive to even minute changes in the power supply voltage, current and frequency. A growing power quality concern is harmonic distortion that is caused by the non-linearity of customer loads. Harmonics distorts the waveform shape of voltage and current level which results in many disturbances. Power electronic converters are widely used in industrialpower conversion systems both for utility and driveapplications.

As the power level increases, the voltage level is increased accordinglytoobtainsatisfactoryefficiency.Themainfunction of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltages. These dcvoltages may or may not be equal to one another. The ac voltage produced from these dc voltages approaches a sinusoid. The staircase waveform produced by themultilevel

inverter contains sharp transitions. From Fourier series theory, this phenomenon results harmonics, in addition he fundamental frequency of the sinusoidal waveform. The harmonics generated on the AC side greatly influence the power quality of the control system. The multi-level inverter improves the AC power quality by performing the power conversioninsmallvoltagestepsleadingtolowerharmonics. Thefloatingvoltagesourcemulti-levelinvertertopologyalso knownasthecascadedmultilevelinverterisoneofthetypical methodsforreducingtheharmonicsbyincreasingtheinverter levels.

II. POWER QUALITYISSUES

A. PowerQuality

Power quality or more specifically a power quality disturbance is generally defined as any change in power (voltage,current,orfrequency)thatinterfereswiththenormal operation of electrical equipment. The IEEE defined power quality disturbances have been organized into seven categoriesbasedonwaveshapeviz:Transients,Interruptions, Sag / under voltage, Swell / Overvoltage Waveform distortion, Voltage fluctuations.

B. Solutions to Power QualityProblems

There are two approaches to the mitigation of power quality problems. The solution to the power quality can be done from customer side or from utility side. First approach is called load conditioning which ensures that the equipment is less sensitive to power disturbances allowing the operation even under significant voltage distortion. The other solution is toinstalllineconditioningsystemsthatsuppressorcounteracts thepowersystemdisturbances.Forlowervoltagesagstheload voltage magnitude can be corrected by injecting only reactive power into the system. However, for higher voltage sags injection of active power in addition to reactive power is essential to correct the voltage magnitude. DSTATCOM is capable of generating or absorbing reactive power but the active power injection of the device must be provided by an external energy source or energystorage system. The response time of DSTATCOM is very short and is limited by the power electronics devices. The expected responsetimeisabout25mswhichismuchlessthansomeof the traditional methods of voltage correction such as tap

changingtransformers.

III. DSTATCOMOPERATION

The basic operating configuration of a DSTATCOM is shown in Fig 1. It consists of a voltage source inverter (VSI), dc side equivalent capacitor (C) with voltage vdc on it and a coupling reactor (Lc). The ac voltage difference across the coupling reactor produces reactive power exchange between DSTATCOM and the power system load bus at the point of common coupling (PCC). If the output voltage of the DSTATCOM (vc) is more than the system bus voltage (vI), reactive power is supplied to the power system and reactive powergoestoDSTATCOMifvcislessthanthatofvI.Totake effect of this bidirectional flow of reactive power, the STATCOM output voltage should be varied according to requirement of reactive powercompensation.

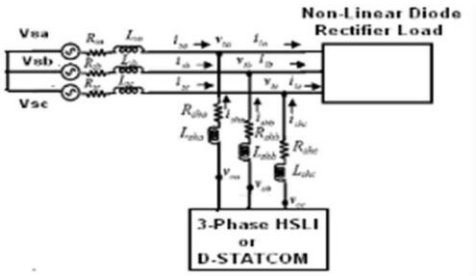


Fig. 1 Basic DSTATCOM configuration.

IV. CASCADEDMULTILEVELINVERTER

TheCMLIconsistsofanumberofH-bridgeinverterunits with separate dc source for each unit and is connected in cascaded or series as shown in Fig 2. Each H- Bridge can produce three different voltage levels Vdc, 0 and -Vdc by connecting the DC source to ac output side by different combination of four switches S1, S2, S3 and S4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridgeoutputs.

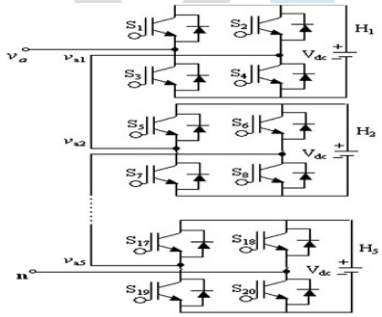


Fig 2 Configuration of single phase N-level CMLI

By connecting the sufficient number of H bridges in cascade and using proper modulation scheme nearly sinusoidal output voltage waveform can be synthesized. The numberoflevelsintheoutputphasevoltageisgivenas2M+1. Where M is the number of H bridges used perphase.

A. Switching anglesselection

Tosynthesizemultilevelacoutputvoltageusingdifferentlevels of dc inputs, the semiconductor devices must be switched on andoffinsuchawaythatdesiredfundamentalvoltageobtained is nearly sinusoidal i.e. having minimum harmonic distortions. Different switching techniques are available for computing switching angles for the semiconductor devices. For power system applications, generally fundamental frequency switching scheme is considered most suitable. In this scheme thedevicesareswitchedonandoffonceineverycycle,thereby producing less switching angles at fundamental frequency are computed by solving a set of nonlinear equations known as selective harmonic elimination (SHE) equations. In SHE technique in general, lower order harmonics are eliminated at the cost of generation of higher order harmonics thereby increasing the total harmonic distortion (THD) in vc. In the presentworkanoptimizationtechniqueisusedforcomputation of switching angles which minimize THD due to all harmonic components up to 49^{th}order.

Significant amount of THD reduction can be achieved as comparedtoSHEtechnique.IngeneraltheTHDinpercentage is definedas

$$THD(\%) = 100 \times \sqrt{\sum_{n=3,5,7,\dots} V_n^2 / V_1} \quad (1)$$ where

$$V_n = 4V_{dc}\left(cos(n\propto_1) + \cdots + cos(n\propto_s)\right)/n\pi$$

B. Capacitor chargebalance

1. One major issue associated with CMLI is the problem of maintaining equal voltage across capacitors connected in differentH-bridges.
2. To rectify this problem, a switch angle rotational scheme is implemented in which switching angles for H-bridge are changed in order after every half cycle so that average conduction period of each H bridge remains same over five half cycles. There are several methods to extract the harmonic components from the detected three-phase waveforms. Among them, the socalled p - q theory based on time domain has been widely applied to the harmonic extraction circuit. The detected three-phase voltage is transformed into the D– Q coordinates by using abc- dq0 transformation. It computes the direct axis V_d, quadratic axis V_q and zero sequence quantities V_o in two axis rotating reference frame. Then by using dq0- abc transformation it transforms three quantities (direct axis, quadratic axis and zero sequence components) from three phase quantitiesexpressedinatwoaxisreferenceframeback toreference.Theobtainedcurrentreferenceisconverted three phase current reference by inverse D – Q transformationI_{ca},I_{cb},and I_{cc} . The three3-$reference compensating currents are compared withthe DSTATCOM compensating currents extracted from ac system.
3. Thus three phase compensating current I_{ca}, $I_{cb}$and I_{cc} are produced. The obtained reference current is given to a PI controller in order to generate controlled gate signal forDSTATCOM.

A. DC bus voltagecontrol

A DC bus controller is required to regulate the DC bus voltage V_{dc} and to compensate the inverter losses as shown in Fig.3. The measured DC bus voltage Vdc of each phase is compared with its reference value V_{dc}*. Similarlyfortheremainingphasesandaddedalltheerror signals. The resulting error is applied to a PI regulator. Theproportionalandintegralgainsaresetto0.12$fi^{-1}$and 0.008 fi^{-1} s^{-1} respectively. Moreover, the DSTATCOM can build up and regulate the DC capacitor voltage.

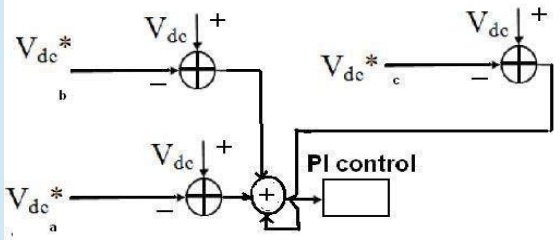
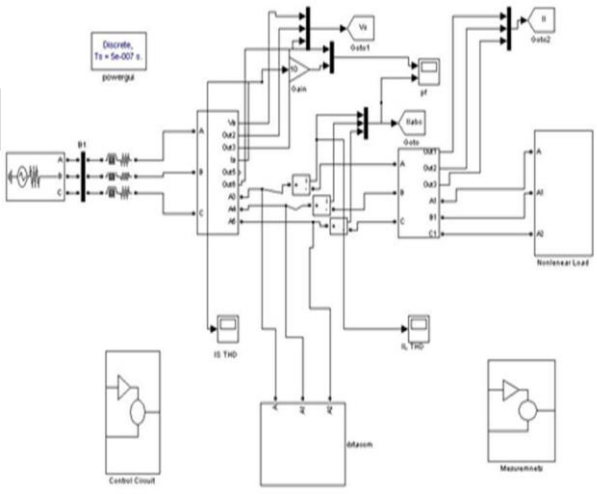


Fig 3. DC bus regulator using PI controller

V. SIMULATION &RESULTS

The performances of DSTATCOM with proposed control schemes are evaluated in Matlab/Simulink software platform. The



Matlab/Simulink model of proposed system with control method is depicted.

Fig.4 Simulation model with D-STATCOM

Fig 5 shows the three phase source voltages, three phase source currents and load currents respectively without DSTACOM. It is clear that without DSTATCOM load current and source currents are same. The system parameters for simulation study are source voltage of 11kv, 50 Hz AC supply, DC bus capacitance 1550e-6 F, Inverter series inductance10mH,Sourceresistanceof0.1ohmandinductance of0.9mH.Loadresistanceandinductancearechosenas30mH and 60 ohms

respectively. Fig 6 shows the harmonic spectrum of phase-A source current without DSTATCOM. The THD of source currentwithout
DSTATCOM is 28.28%. Fig.7 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOMeventhoughloadcurrentisnon-sinusoidalsource currents aresinusoidal.

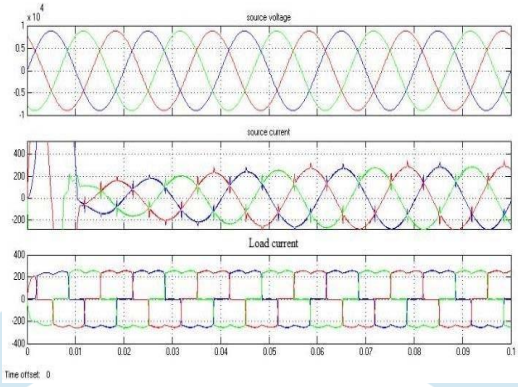


Fig. 5 Source voltage, current and load current without DSTATCOM

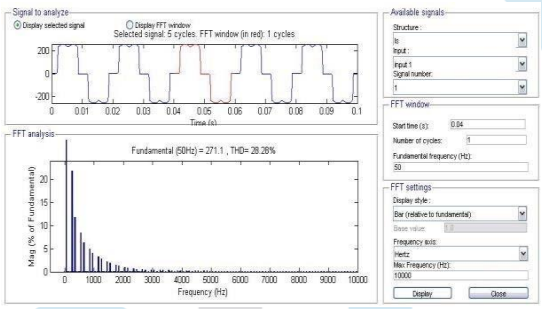


Fig. 6 Harmonic spectrum of Phase-A Source current without *DSTATCOM*

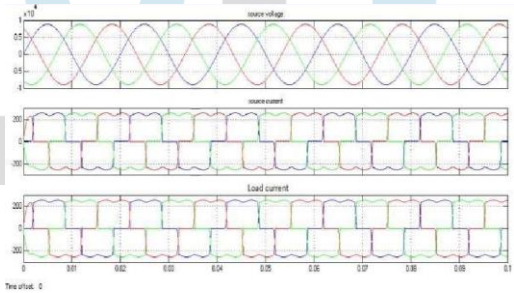


Fig. 7 Source voltage, current and load current with DSTATCOM

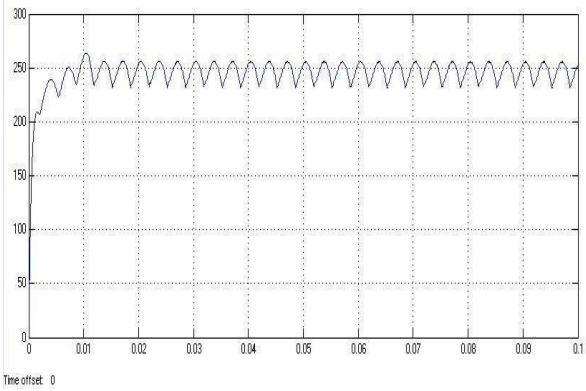


Fig. 8. DC bus voltage

Fig.8.shows the DC Bus voltage which is maintained at constant voltage. Fig.9. shows the phase-A source voltage and current even though the load is non linear RL load the source power factor is unity.

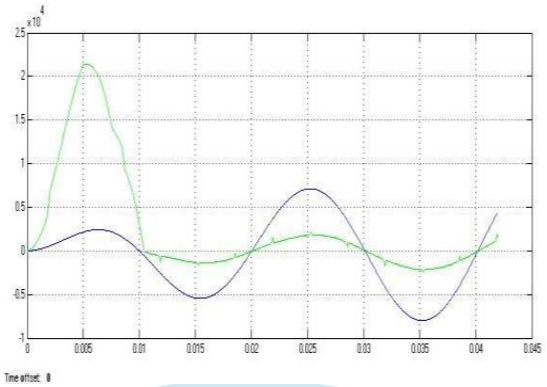


Fig.9. Phase-A source voltage and current and pf

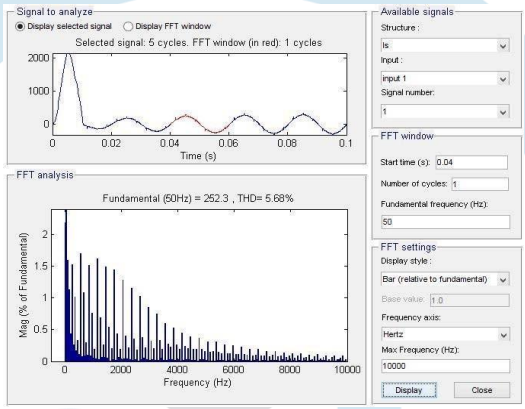


Fig. 10 Harmonic spectrum of phase-A source current with DSTATCOM

Fig.10 shows the harmonic spectrum of Phase –A Source current with DSTATCOM.

VI. CONCLUSION

In this paper a Transformer less Based Modified Cascaded Five-Level (TBMCSL) H – bridge Inverter is used as a DSTATCOM in Power System and is successfully demonstrated in MatLab/Simulink. The benefits of TBMCSL H – bridge Inverter has low harmonics distortion, reduced number of switches to achieve the five- level inverter and reduced switching losses. The source voltage, load voltage, sourcecurrent,loadcurrentandpowerfactorsimulationresults under nonlinear loads are presented. The TBMCSL H – bridge Inverter is installed on a power distribution system with focus on harmonic reduction and voltage regulation performances. Harmonics present in the distribution system are significantly reduced by TBMCSL H – bridge Inverter. The results were showed good for dc bus voltage – regulation, reduced source harmonic currents and have stableoperation.

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