A New Low Power High Speed Modified ONOFIC Approach in DSM Technology

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***Abstract*:- Since the last two decades, the trend of device miniaturization has increased to get better performance with a smaller area of the logic functions. In deep submicron regime, the demand of fabrication of nanoscale Complementary metal oxide semiconductor (CMOS) VLSI circuits has increased due to evaluation of modern successful portable systems. Leakage power dissipation and reliability issues are major concerns in deep submicron regime for VLSI chip designers. Power supply voltage has been scaled down to maintain the performance yield in future deep submicron regime. The threshold voltage is the critical parameter to trade-of the performance yield and leakage power dissipation in nanoscaled devices. The simulation results on Synopsys HSPIC at 45nm and 32nm technology at 10 MHz frequency. Proposed leakage reduction technique provides 40% reduction in leakage over the existing leakage reduction technique in the literature.**

***Keywords*: Leakage current; stacking; MTCMOS; dual threshold CMOS, ONOFIC.**

I. Introduction

Modern device dimensions have been scaled down since the last two decades and the number of transistors on a chip has thus increased to integrate more applications in a small area. Device miniaturization increases the device density on single silicon buffer and reduces the propagation delay. Switching speed of the CMOS circuit is inversely proportional to the delay of that logic circuit. Equation (1) shows that the threshold voltage of the device must be reduced proportionally by reducing the supply voltage of the device so that it should maintain the performance of the device. However, the main component of the leakage current called subthreshold, increases exponentially when the threshold voltage of the device is reduced. Subthreshold leakage current of the device.

V_T is the thermal equivalent voltage, $V_T = kT/q$; V_{TH} is the threshold voltage of the device, COX is the gate oxide capacitance, μ is the mobility factor, m is subthreshold swing coefficient and CDM is the capacitance of depletion layer. Leakage current increases dramatically with each new technology generation.6 Each new microprocessor chip generation increases a 7.5x in the leakage current and a 5x in total energy dissipation.7 As leakage current is increasing drastically with technology scaling, it will become the most effective part of total power dissipation. There are four sources of power dissipation in CMOS circuits; dynamic power, short circuit power, leakage power and static bias power. Generally, dynamic power is the dominant component and other three parts are negligible at above deep submicron technologies. But leakage power is the dominant component of total power dissipation at below deep submicron technologies. Total power dissipation of the logic circuit.

This paper proposes a novel leakage reduction technique that reduces leakage significantly without much overhead in power/area and performance. The simulation results shows that proposed approach of leakage reduction provides significant reduction in leakage current over the existing technique. Thus, proposed method of leakage reduction can be effectively utilized in portable devices.

II. SOURCES OF LEAKAGE AND DIFFERENT LEAKAGE REDUCTION TECHNIQUES

Significant efforts have been devoted to reduce leakage. Before getting detailed discussion on the different leakage reduction techniques, the first subsection shows different sources of leakage in the VLSI chips.

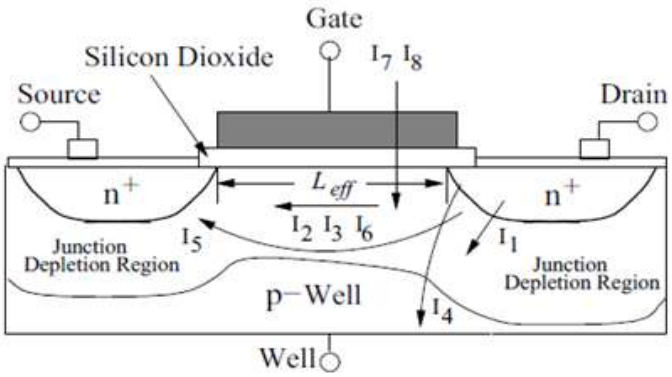

Fig.1. Leakage Mechanism in Short-Channel NMOS Transistor

2.1 Sources of Leakage:

The static power dissipation can be calculated by the product of the leakage current flowing in the device and the supply voltage:

$$P_s = i_{leakage} * V_{dd}$$

There are six major sources of leakage in the sub-nanometer MOS device as shown in Figure 1. Figure1: Sources of leakage in a transistor From the figure it can be seen that I1 is the reverse bias pn-junction leakage current whereas I2 is the sub-threshold leakage. It is current drain-to-source current flows while the gate is biased below threshold voltage. I3 is the oxide tunneling current which arises
due to large electric field and can be overcome by considering high-K material. I4 represents leakage due to hot carrier injection whereas I5 is gate induced drain leakage. Finally the I6 represent punch through current which is excessive and may burn out the transistor.

2.2 Leakage Reduction Techniques:

This section details different leakage reduction techniques.

2.2.1 Transistor Stacking [5]: The sub-threshold current in the transistor reduces significantly when
two or more transistor in series is in off condition. In this condition, source voltage of the stacked transistor increases that reduces, gate-to-source (VGS) voltage, drain-to-source (VDS) voltage and increases the body reverse biasing voltage (VBS) as shown in Figure 2. Figure 2: Illustration of ransistor stacking All these effects result in significant reduction in the leakage current. In order to further reduce the leakage, more number of the series connected transistors are applied the input that made them turned off. The approach is sometimes called as forced stack technique.

2.2.2 Dual Threshold

In this technique transistors which are in non-critical path are kept at higher threshold to reduce the leakage whereas the transistors in critical path fabricated with low threshold as shown in Figure 3. The lower threshold in the critical path reduces the delay of the design whereas higher threshold on non-critical path allows lower leakage of the circuit. Thus the dual threshold technique provides lower leakage without disturbing the performance of the design.

LECTOR Technique [7]:

The Leakage Control transisTOR (LECTOR) technique uses two leakage control transistors (LCTs) (a PMOS and an NMOS) in CMOS logic as shown in Figure 5. In this approach, each LCT transistor is controlled by the other LCT. Since one of the LCT is always near its cut-off for any combination of input signal, it decreases current in the path from VDD to ground. LECTOR is single threshold, an input pattern independent scheme which inserts two transistors in the path between pull-up and pull-down logic circuit. The concept of LECTOR technique is an application of transistors stack in the path from the power supply to ground. When one or more transistors are in cut-off mode then they behave as large value resistance and mitigate the leakage current. LECTOR is capable to reduce leakage current in both active and standby modes.

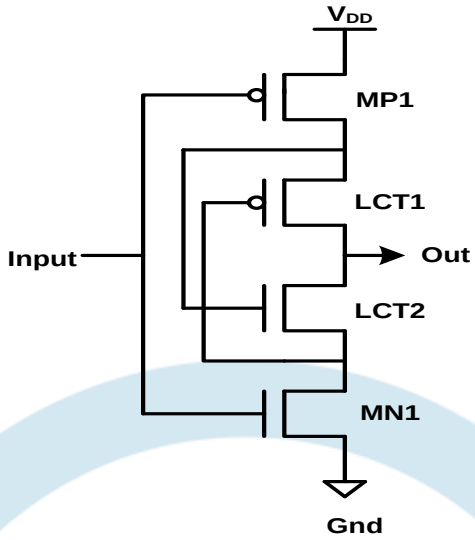

Fig.2. LECTOR based NOT Gate

III. Proposed Circuit

In this section a novel designe are introduced namely modified ONOFIC approach with and sleep transistor at Header and Footer known as power gated technique. These are the combinations of self controlling and external leakage controlling technique. In self controlling technique no external signals are applied while in external leakage controlling technique external sleep signal are applied which switches OFF the sleep transistor to reduces the leakage power. The basic idea behind all the proposed techniques is to provide stacking effect of the transistor which mitigates leakage power from V_{dd} to GND as shown in Figure.3.

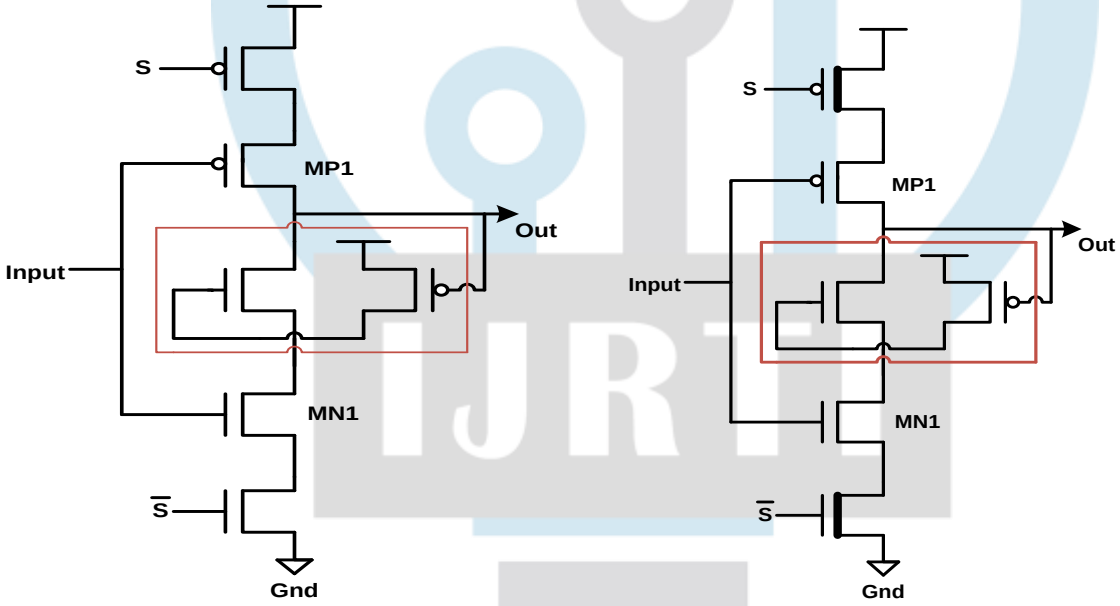

Fig.3. (a) Proposed Modified ONOFIC with Low V_{th} (b) ONOFIC with high V_{th}

IV. Results and Discussion

This now work on Conventional gate circuits designing has been carried out with the sole purpose of achieving even better performance of devices. And that performance is being evaluated based on certain performance evaluation parameters. In over work we have calculated various parameters on conventional and proposed techniques on various gates, from simulation results proposed circuit saved dynamic power, static power, delay and PDP than other existing techniques. All the existing and proposed technique are simulated in HSPICE at 32nm technology with supply voltage of 0.9V, output capacitance C_L =1pF, Leakage power is investigate at different temperature at 25^0C and 110^0C, The size (W/L) of all existing and proposed circuit made from P-MOS and N-MOS is same for fair comparison of results

Table.I. Calculation of Average Power, Delay, PDP and EDP at 45nm

	Average Power (µW)	Delay (pS)	PDP(aS)	EDP(E-30)
Conventional Inverter	1.285	47.10	60.52	2850
Conventional NAND Gate	0.891	56.29	50.15	2822
Conventional NOR Gate	0.630	23.76	14.96	355.4
LECTOR Inverter	0.533	65.48	34.90	2285
LECTOR NAND Gate	0.719	69.29	49.81	3451
LECTOR NOR Gate	0.429	22.37	9.596	214.6
ON OFF Inverter	0.283	57.36	16.23	930.9
ON OFF NAND Gate	0.794	62.29	49.45	3078
ON OFF NOR Gate	0.583	16.37	9.543	156.2
Proposed ON OFF NAND Gate	0.463	58.38	27.02	1577

Table.II. Calculation of Average Power, Delay, PDP and EDP at 32nm

	Average Power (µW)	Delay (pS)	PDP(aS)	EDP(E-30)
Conventional Inverter	2.385	36.23	86.40	3130
Conventional NAND Gate	1.683	45.26	76.17	3447
Conventional NOR Gate	1.432	13.83	19.80	273.8
LECTOR Inverter	1.354	54.92	74.38	4084
LECTOR NAND Gate	1.479	57.84	85.37	4937
LECTOR NOR Gate	1.225	13.94	17.07	237.9
ON OFF Inverter	1.197	49.38	59.10	2918
ON OFF NAND Gate	1.583	53.38	84.50	4510
ON OFF NOR Gate	1.386	12.37	17.14	212.0
Proposed ON OFF NAND Gate	1.029	46.49	47.83	2223

Table.III. Leakage power and delay of LCT NAND gate and basic NAND GATE, Process technology 180 nm, supply voltage = 1.8 Parameters

Parameters	Temp	Leakage Power		
		Basic NAND Gates	LCT NAND Gate	Proposed NAND Gate
Temp Variation (^{0}C) at supply Voltage 1.8V	7^0C	4.048E-08	3.012E-08	2.098E-09
	27^0C	1.456E-07	1.108E-07	9.012E-09
	47^0C	4.464E-07	3.465E-07	3.224E-08
	67^0C	1.197E-06	9.462E-07	9.921E-08
	87^0C	2.872E-06	2.305E-06	2.690E-07
Supply Voltage Variation at 25^0C	1V	3.863E-08	2.260E-08	6.744E-09
	1.2V	5.944E-08	3.587E-08	7.071E-09
	1.4V	8.458E-08	5.552E-08	7.354E-09
	1.6V	1.098E-07	8.445E-08	7.613E-09
	1.8V	1.291E-07	1.267E-07	7.859E-09

For Validation and Verification Circuit is implemented on Full Adder Circuits

One Bit FULL ADDER Circuit (1 Bit FA)

One Bit ADDER circuit implemented by two cascaded Ex-OR circuit and one NAND gate which outputs gives SUM and Carry signal respectively. The circuit of 1Bit FA is shown in Fig. 4.

(i) Circuit Diagram

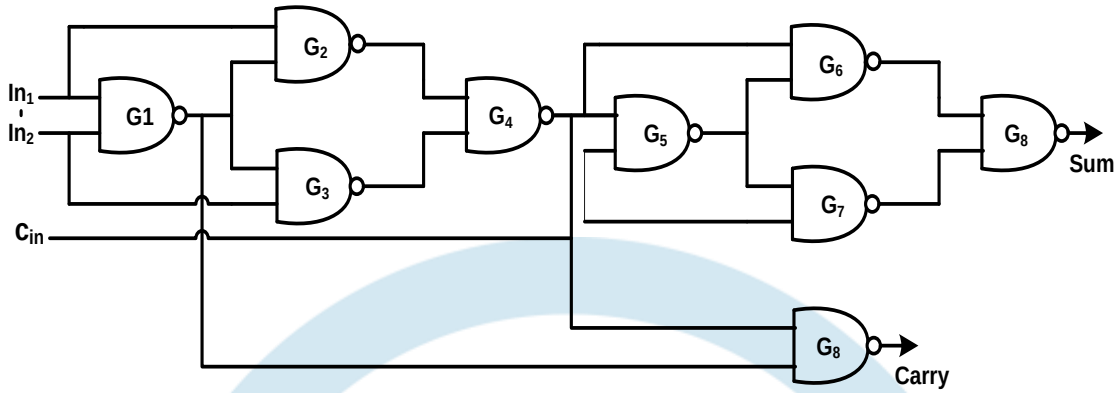

Fig.4. One Bit FULL ADDER (1 Bit FA) Circuit

Table.IV. P_{ST}, P_D, P_T of all basic gates and Adders in existing and proposed circuits

Logic	P_{ST}(nW) + P_D (uW) = P_T(uW) Original Circuit	P_{ST}(nW) + P_D (uW) = P_T(uW) ONOFIC Circuit	P_{ST}(nW) + P_D (uW) = P_T(uW) Proposed Circuit
NAND	27 + 0.19=0.22	15.3+0.17=.19	3.76+0.12=0.12
OR	28 + 0.65=0.68	16.5+0.63=.65	4.9+0.52=0.52
AND	27.5 + 0.48=0.51	15.9+0.47=.49	4.33+0.42=0.42
Ex-OR	40.5 + 1.1=1.14	28.9+1.02=1.05	17.35+0.61=0.63
Ex-NOR	41 + 1.44=1.48	29.5+1.39=1.42	17.92+0.65=0.67
1bitFA	108 + 1.66=1.77	73.1+1.4=1.47	38.5+1.2=1.24
2 Bit FA	215.9 + 3.12=3.34	146.3+2.98=3.13	76.96+2.57=2.65
4 Bit FA	431.8 + 6.34=6.77	292.6+6.2=6.49	154+5.3=5.45

V. Conclusion

Leakage reduction solution as compared with the other conventional and relevant techniques and there is no need of technology modification, no change of fan-out logic state of WLS gates during idle mode and needs no additional power supply. Trade–off between area, delay and power requirements can be obtained by the use of specific variant in a given circuitAnd every variants suitable for specific performance parameter like V1, and V2 is better when speed is our main concern, it reduces 14.58% of the average delay for these circuits, but in this case W/L ration of PMOS must be adjust. Table.I and II shows overall optimum result for leakage reduction and power.

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