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Comparative Analysis of Efficient Designs of D-Latch using 32nm CMOS Technology

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***ABSTRACT*: In this paper we have proposed various efficient designs of low power D-latch using 32nm CMOS technology. We have designed and simulated these circuits in HSpice simulation tool. In this simulation we have modified W/L ratio of each transistor in each circuit. We have taken power supply of 0.9V. We have calculated average power consumed propagation delay and power delay product.**

***Keywords*: Latch, CMOS, Clock, Power Delay Product, MOSFET**

1. INTRODUCTION

Developments in large scale integration resulted in millions of transistors placed on a single chip for execution of intricate circuitry. Due to this placing of large no of transistors within a small area resulted in more heat dissipation and power consumption. To solve these problems many research were carried on and solutions were proposed such as by decreasing the power supply voltage, switching frequency and capacitance of transistor. Maximum number of VLSI related applications such as DSP, image & video processing and microprocessors, widely uses logic gates and arithmetic circuits. Operations such as AND, OR, addition, subtraction, and multiplication are usually used by these circuits. The building blocks of maximum digital circuits are logic gates, whereas in arithmetic circuits, 1-bit full adder cell is widely used. Therefore improving their execution is vital for improving the overall module performance. Due to fast development in mobile communication and computation technology demand for building of low-power VLSI systems has come forth. The technology related to battery does not progress at the same rate as that of microelectronics. Thus for the mobile systems a fixed amount of power is available. Thus, more constraints are being faced by the engineers such as: high speed, high throughput, small silicon area, and at the same time, low-power consumption. Therefore great interest was shown for designing of low-power, high performance adder cells.

Limitation due to power dissipation can be represented by two methods. The former one is related to cooling while realizing high performance systems. Large amount of energy is dissipated from high-speed circuits in a short amount of time resulting in significant amount of heat. The produced heat requires to be removed from the package on which integrated circuits are attached. If the package cannot amply disperse this heat or if the requisite thermal components are too costly for the application heat removal may become a limiting factor. The later one relates to failure of high-power circuits due to the growing acceptance of portable electronic devices. Batteries are used as a power source in applications such as Laptop computers, portable video players and cellular phones. These devices require recharging after being operational for a limited time of operation. To lengthen the battery life, low power procedure is necessary in integrated circuits.

2. D-LATCH

The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. The D-latch whose waveforms are shown in Figure 1 is such a device: it is a memory element having at least two inputs, namely a clock signal {CLK) and a data signal (D) and an output (Q) (and often its complement). The device is ‘transparent' during one of the clock levels the transparent phase during which the output Q follows the input D. But when the clock level is complemented to its isolation phase the logic level present at D is frozen at Q, which remains in that state until CLK returns to its transparent phase. D-latches are categorized as being ‘positive' or ‘negative’, depending upon the logic level of the transparent phase.

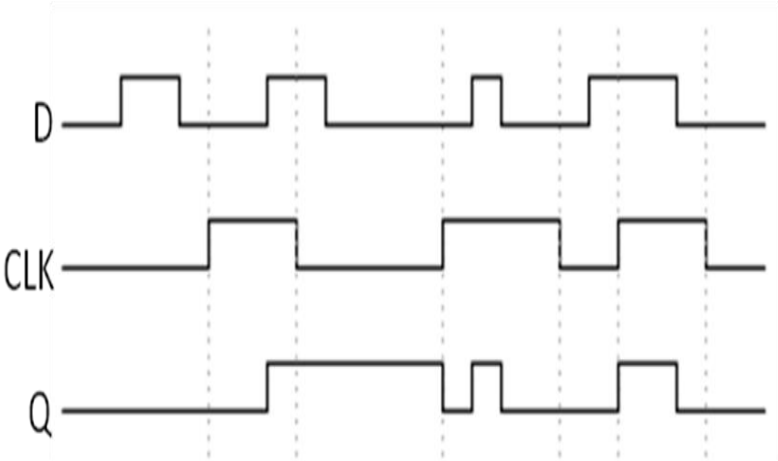

Fig 1 D-latch waveform

3. PROPOSED WORK

We have designed six types of efficient circuit of D-Latch using MOSFET which consumes less average power. All circuits are designed using 32nm CMOS technology at 5 GHz. Power supply is 0.9V. All designs are shown below.

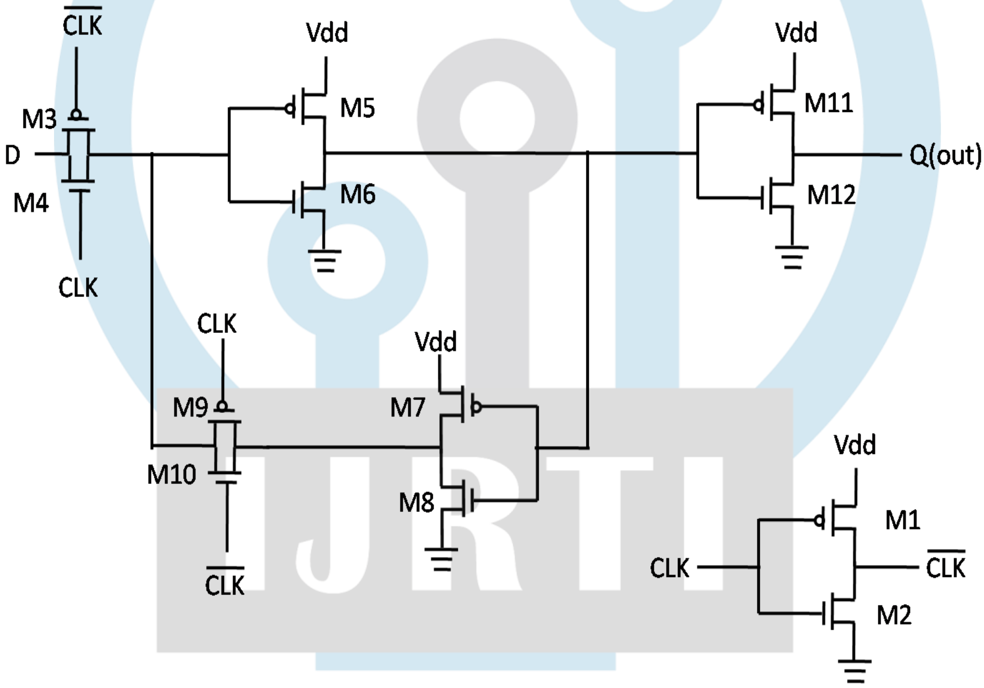

Fig 2 D-latch design 1

From fig. 2, it is the simplest method to demonstrate the working of D-Latch. When clock (CLK) is high mosfets M3 & M4 conduct and passes the input (D) further and M5, M6 invert the data which is again inverted by M11 & M12 to get the same data. At this instant data is stored and latched by M7, M8, M9 & M10. Now if the clock is low, whatever is the input does not pass further, only previous latched data gets passed to the output because of conduction of M9 & M10.

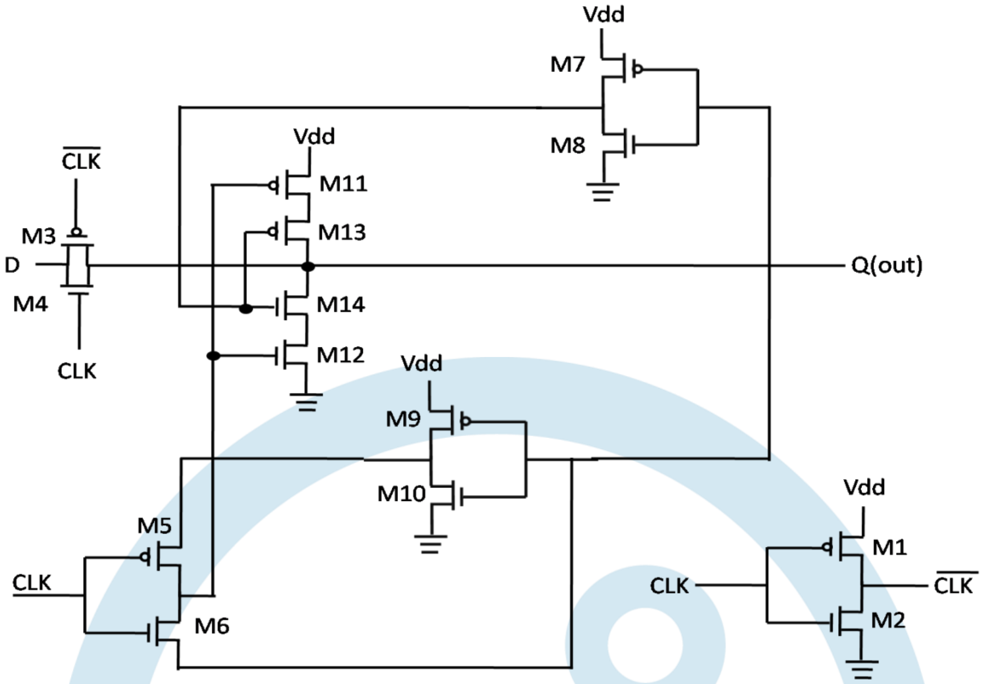

Fig 3 D-latch design 2

From fig. 3, when clock (CLK) is high, M3, M4 conducts and input D passes to the output. This output also goes to M7, M8, M9, M10 and gets inverted. Now if the clock is low, inverted data switches on M11, M13 (if D = '1') & M12, M14 (if D = '0') and keeps the previous data at the output terminal.

Similarly some other circuits of D-latch are also designed using 32nm CMOS library which are shown as follows:

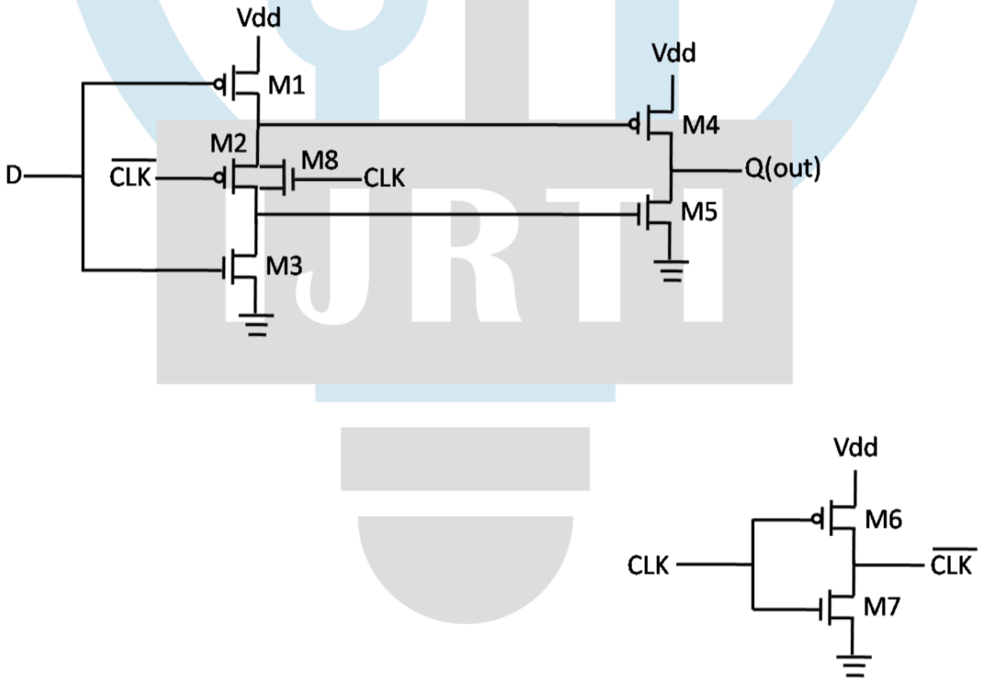

Fig 4 D-latch design 3

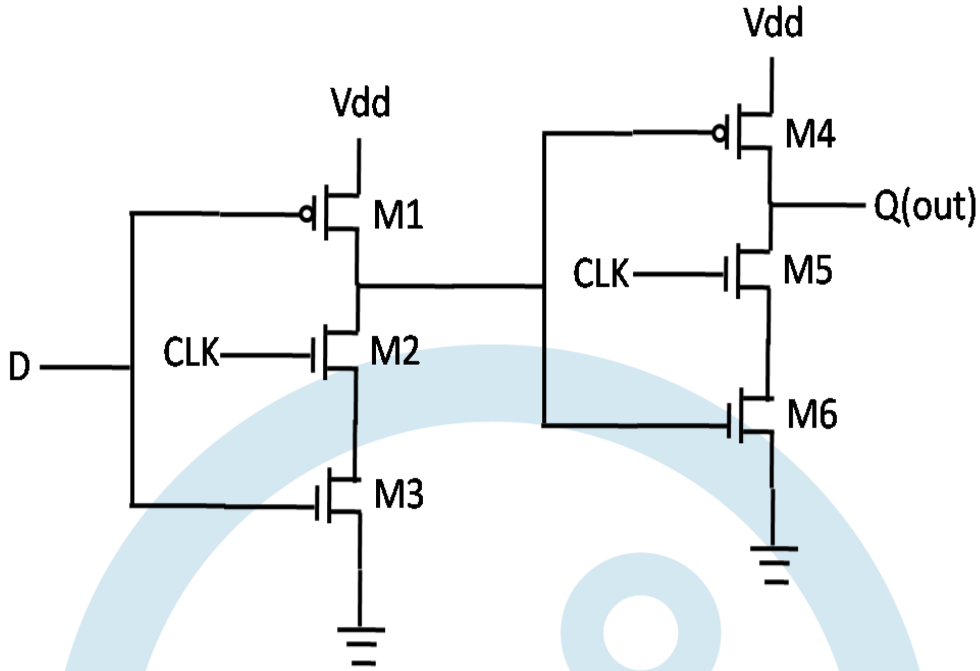

Fig 5 D-latch design 4

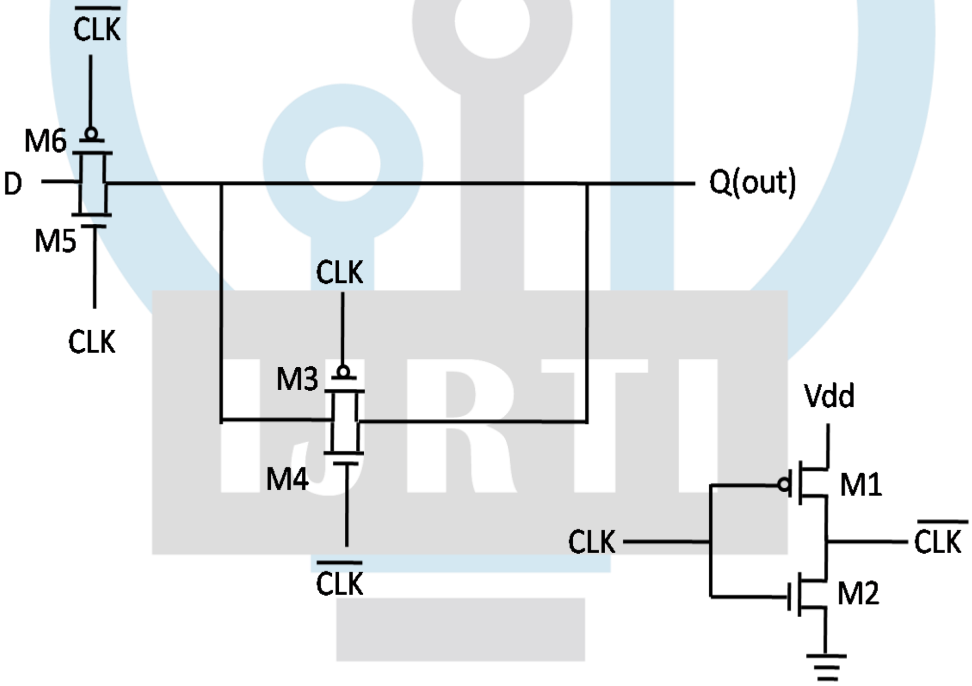

Fig 6 D-latch design 5

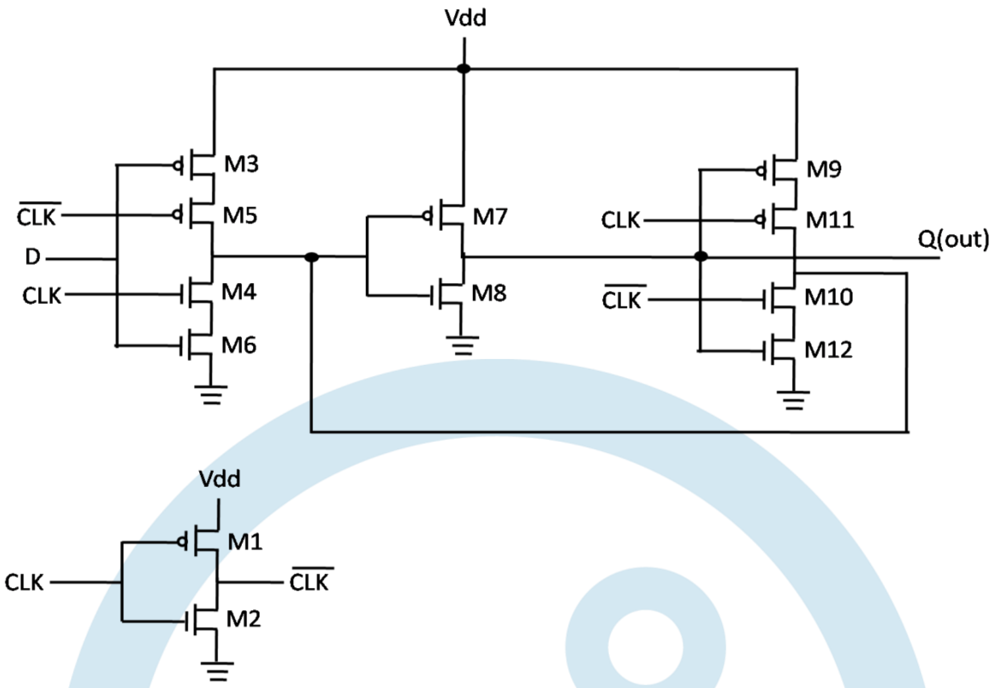

Fig 7 D-latch design 6

4. EXPERIMENTAL RESULTS

Now in this section, we have shown output graphs for each circuit design operated at frequency of 5 GHz. We have provided clock signal of frequency 5 GHz and a data signal to each circuit. Output waveforms are shown as follows:

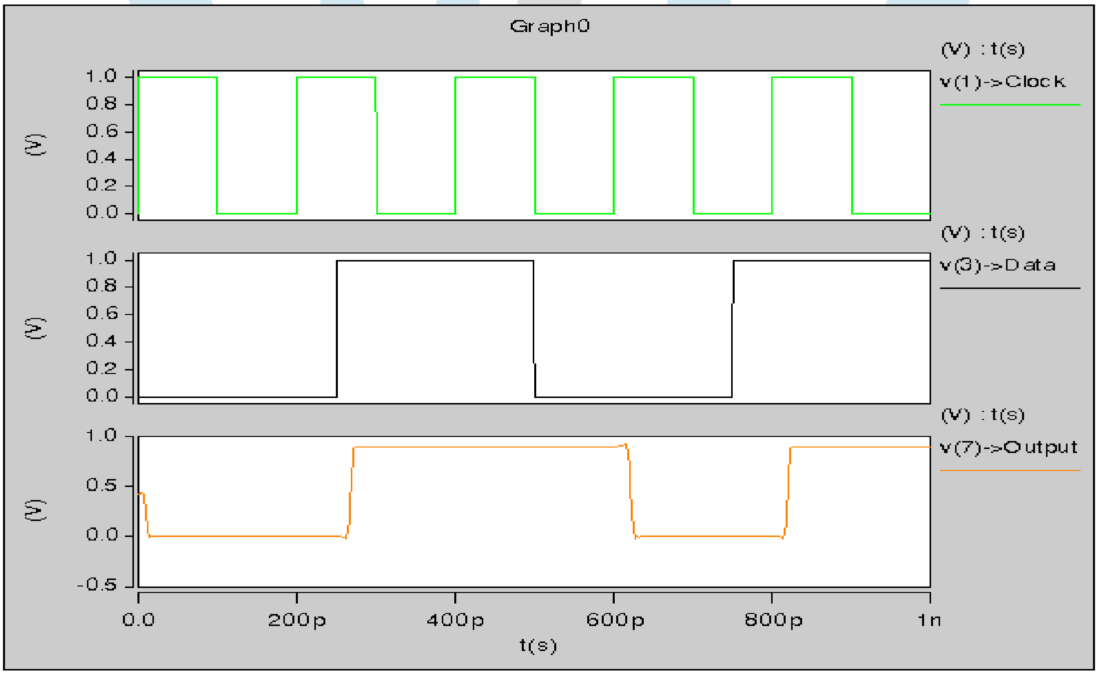

Fig 8 Output of D-latch design 1

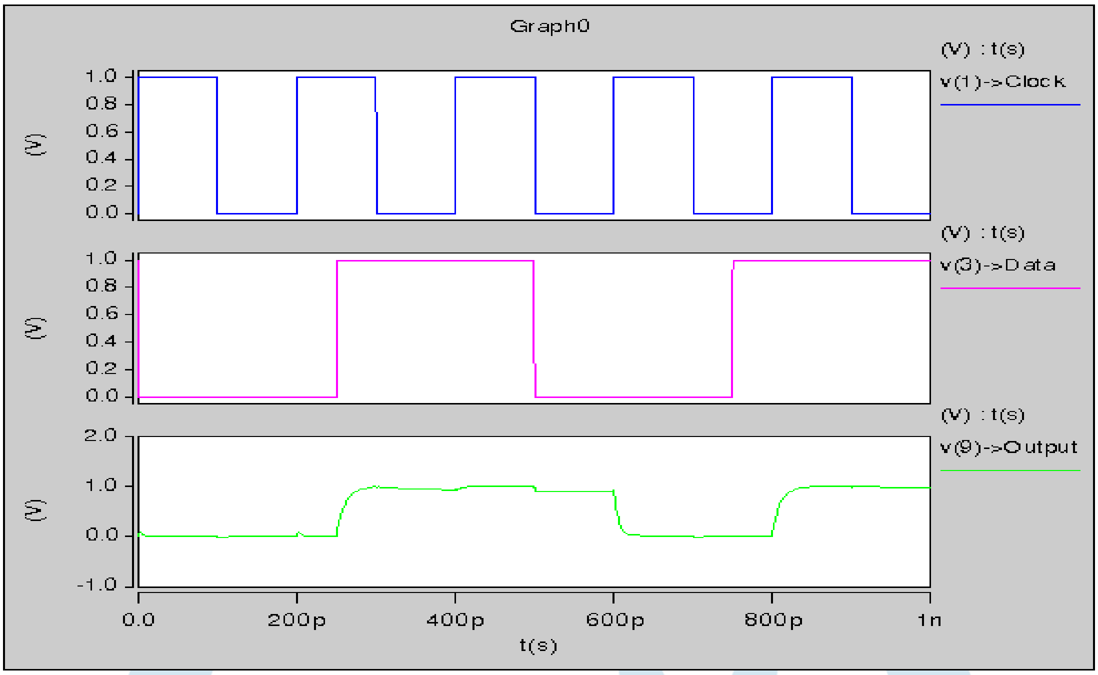

Fig 9 Output of D-latch design 2

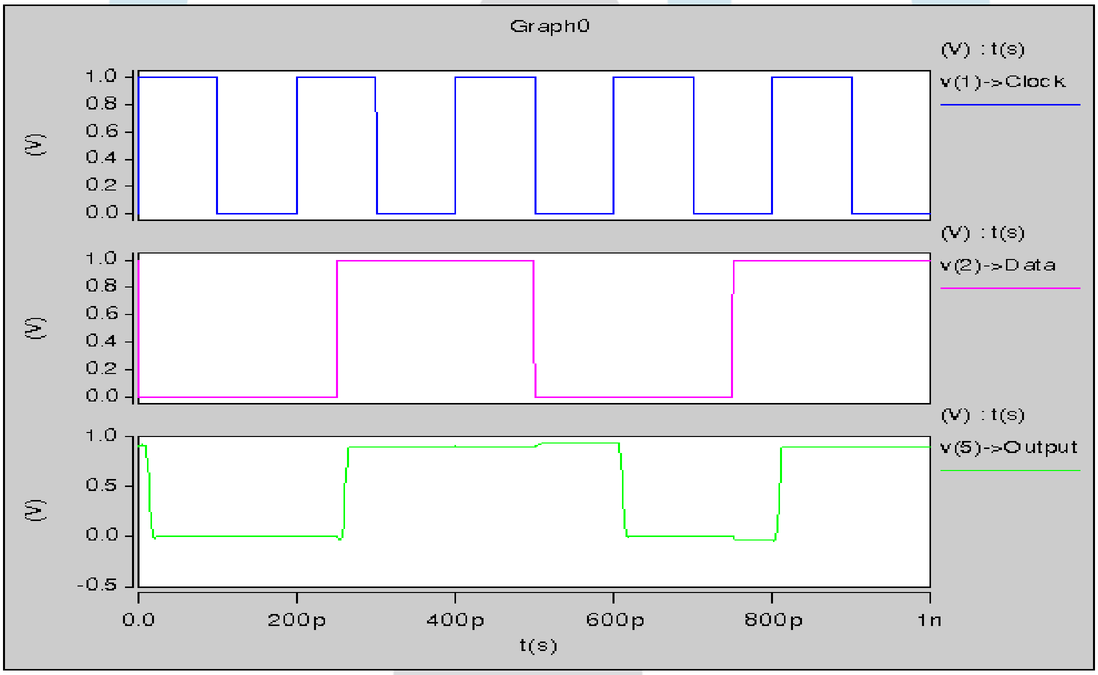

Fig 10 Output of D-latch design 3

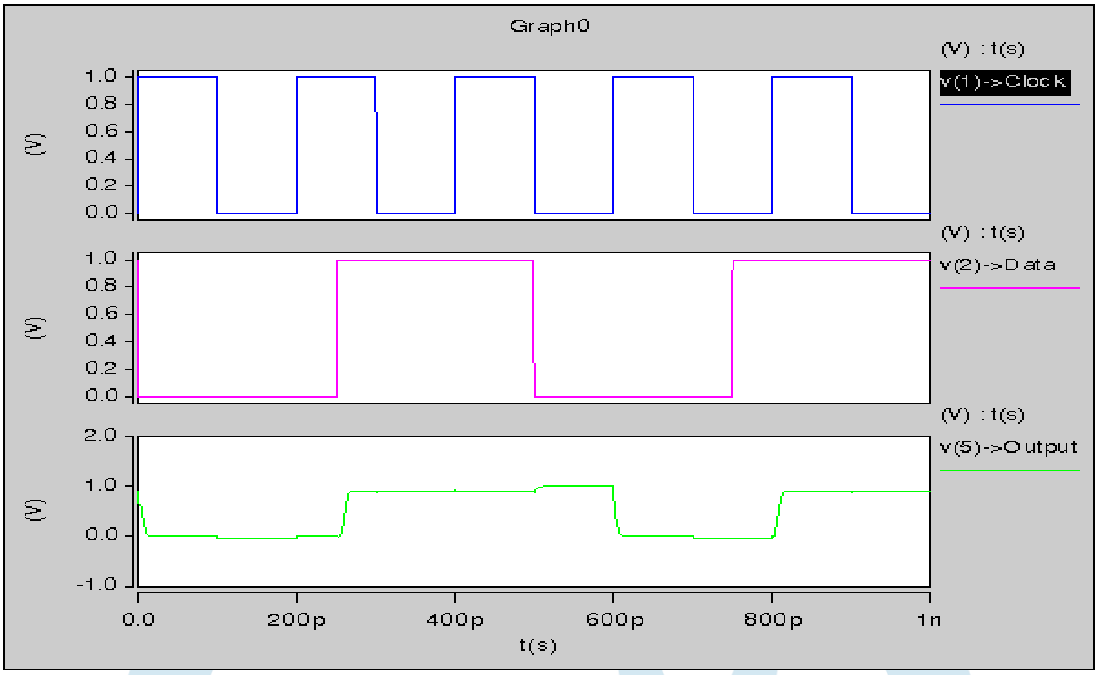

Fig 11 Output of D-latch design 4

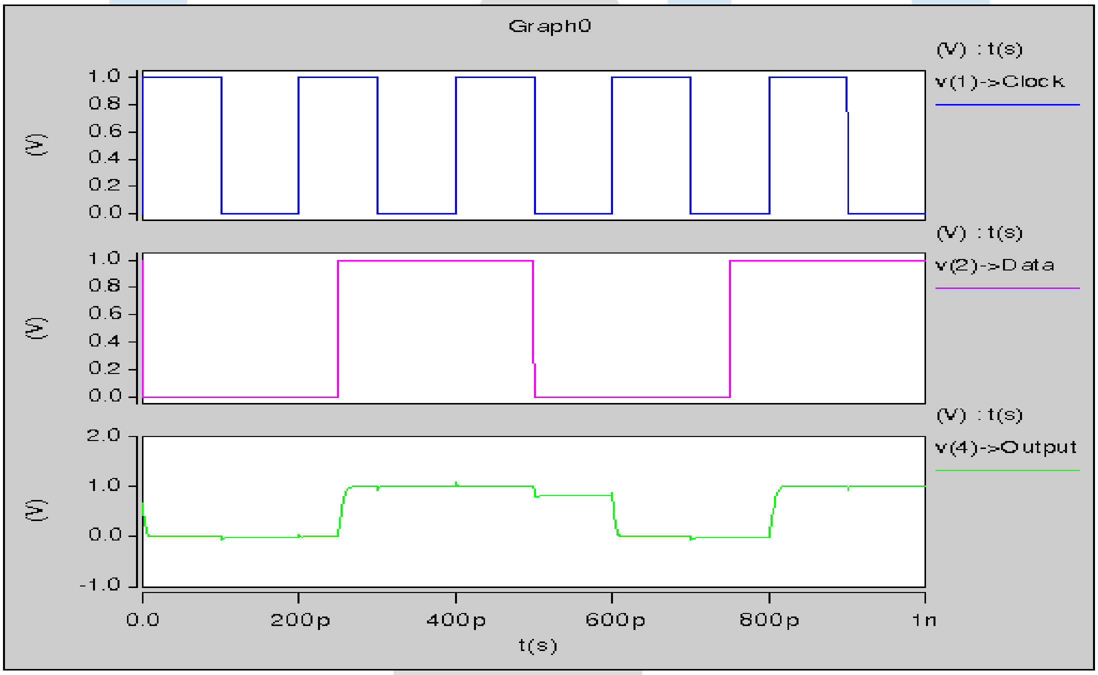

Fig 12 Output of D-latch design 5

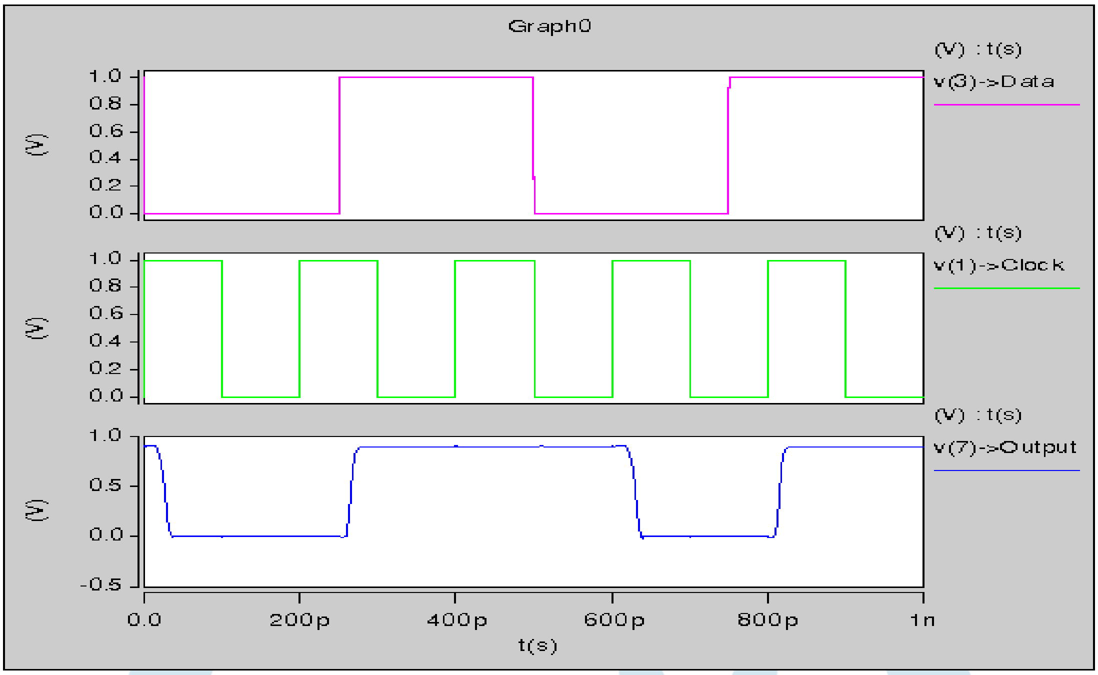

Fig 13 Output of D-latch design 6

Table 1 depicts the comparison between these designs of D-latch according to different parameters. These simulations also show better performance of these circuits as compared to circuits and results described in other literatures.

Table 1: Comparison between designs of D-latch

Design No.	No. of Transistors	Average Power (µW)	Delay Time (ps)	PDP (fJ)
1	12	0.38	319.5	0.12
2	14	0.35	306.04	0.11
3	7	0.13	12.44	0.002
4	6	0.07	8.06	0.006
5	6	0.16	2.44	0.004
6	12	0.26	21.5	0.005
Ref [5]	14	1.05	38.10	0.040

5. CONCLUSIONS

In conclusion, it has been observed that design of D-latch based on sleep transistor shows better performance than stacked inverter. All the simulations are performed n HSpice simulation tool using 32nm CMOS library at power supply of 0.9V for frequency of 5GHz. These designs are working satisfactorily at high frequencies.

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