VEDIC ALU USING AREA OPTIMISED URDHVA TRIYAMBAKAM MULTIPLIER

[1]Utsav Malviya, [2]Gopal Kumar, [3]Vivek Singh Rathore

Assistant Professor,
Government Engineering College, Bilaspur

***Abstract*: Multiplication has some limits and to overcome these limitations a new approach has been describe and designed a vedic multiplier with proposed unique addition structure, which is used to perform addition of partially generated products. To meet main concern 'Speed' and 'area' we have came up with a need particular high speed ALU, the speed of ALU greatly depends upon the speed of multiplication unit used in it. There are so many multiplication techniques exist now a days at algorithmic and structural level. It is been proved that vedic multiplication is the fastest multiplication approach but there are some other multiplication techniques which are batter then vedic multiplication in terms of chip area. Proposed work is a new architecture of 16 bit vedic with combination of 4 bit vedic multiplications and that 4 bit multiplication is been have developed with a unique addition structure. The observed results are been very good and optimized. Later on ALU module is been developed. the tool used for the designing is Xilinx XST and the target platform for validation is Vertex family vertex-4 FPGA, the preferred language is VHDL.**

***Keywords*: CSA carry save adder ALU arithmetic and logical unit, MAC multiply and accumulate unit, RTL register transfer level, UCF user constrain file**

I. INTRODUCTION

Now days we are living in digital world, where all the operations get performed more reliably and with highest accuracy by digital signal processor. ALU is the key element of all these processor like Microprocessor, Microcontroller, DSP processor etc. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. Speed is the most prominent factor of processor and controllers being used recently.

By improving the ALU unit we can develop efficient the Digital Signal Processor, for that proposed Arithmetic unit appears very useful. One of the major purposes of Vedic mathematics is to execute the difficult calculations in simple manner, even orally manageable without much use of pen and paper.

II. PROPOSED ARITHMETIC UNIT

Proposed 16x16 bit Arithmetic Unit is given in the figure 1. Here the A and B are the two 16 bit inputs of proposed Arithmetic Unit. And other part of the design includes Adder, Subtractor, Multiplier, and ALU. Product and Accumulated product are 32 bit output while differences, S are 16 bit output. Proposed work did not focus on the designing of the adder and subtractor circuits as these are not consider modules which consumes large amount of area and power in ALU. But after lots of study it is been found that generally, carry ripple adders can be used when it required to meet timing constraints because they are easy to build and compact.

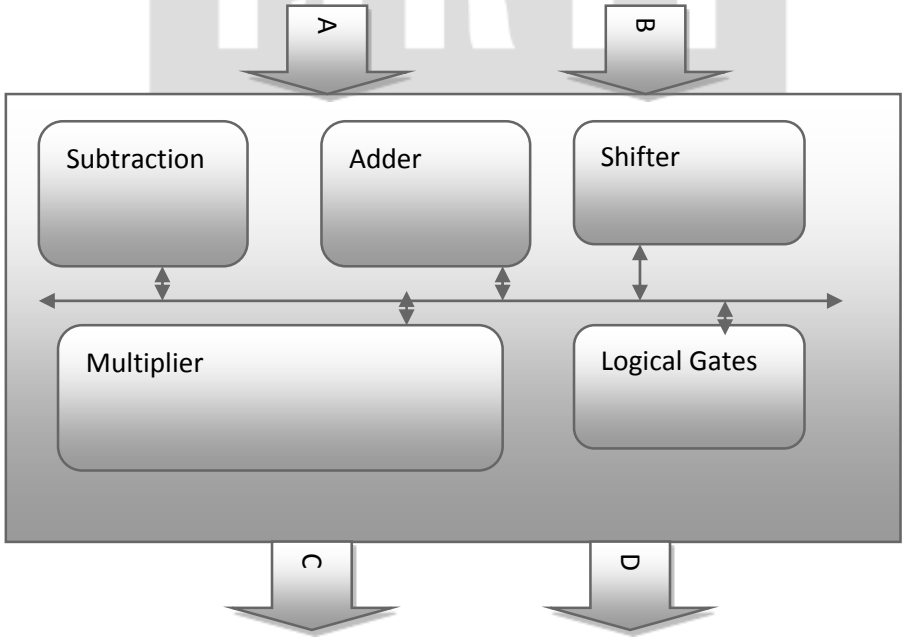

Fig 1.Arithmetic Logic Unit Module

III RESULTS

Till now we have successfully new design for 4 bit vedic multiplier with the help of new addition structure and also design 8x8 and 16x16 with help of 4x4 multiplication. Proposed work is a design of ALU with the help of modified new urdhava triyambakam vedic multiplication method (i. e. proposed multipliers). After successful implementation 4x4, 8x8 and 16x16 an ALU is been design and Figure 2 below shows the simulation results for the ALU design modules and it shows the results for multiplication, subtraction and addition.

Family : Vertex 4 FPGA Family	
Observed results for proposed vedic 4x4	
No of Slices	18
No of 4 input LUT	31
No of bounded IOBs	16
Logical Delay	4.891 ns
Observed results for proposed vedic 8x8	
No of Slices	90
No of 4 input LUT	158
No of bounded IOBs	32
Logical Delay	6.448 ns
Observed results for proposed vedic ALU 16x16	
No of Slices	452
No of 4 input LUT	803
No of bounded IOBs	68
Logical Delay	9.007 ns

Table 1: results observed for design

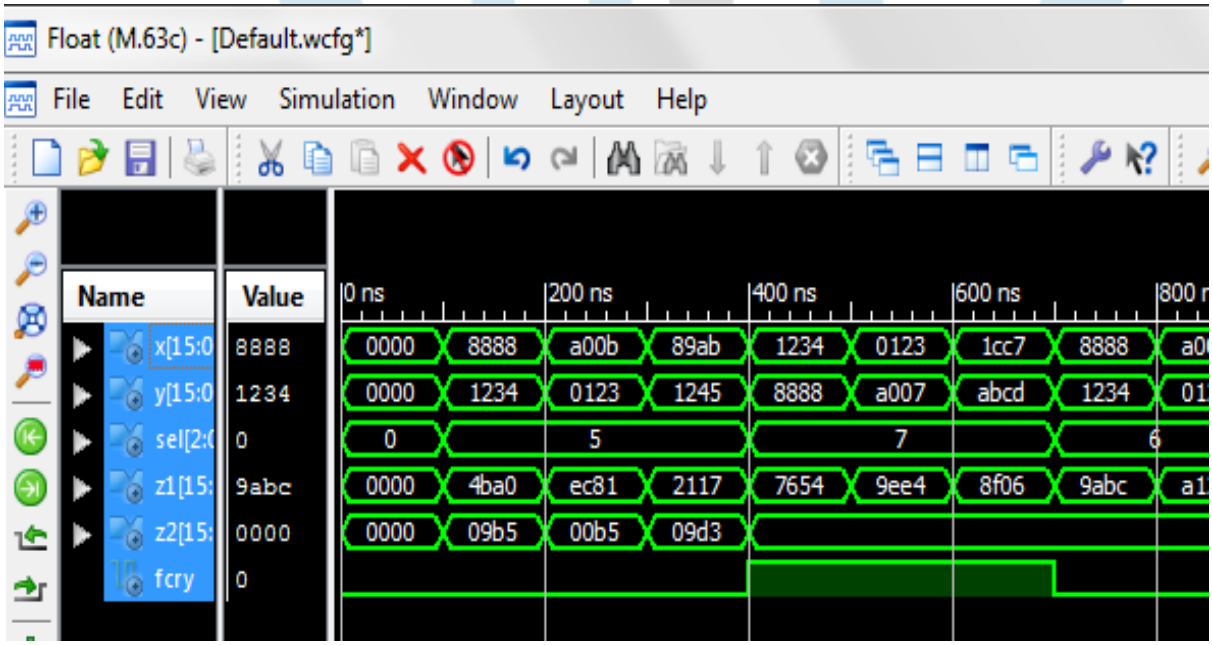

Figure 2: simulation results of ALU

The results are been produced after RTL entry in Xilinx EDA tool. Simulation is done on Xilinx ISE and results are been verified correctly.

Platform used is vertex family FPGA			
Design	**Logical Delay**	**Slice**	**LUT**
Proposed Vedic 4 bit	4.891 ns	18	31
Base 1 (4x4)	8.387	19	-
Base 2(4x4)	-	-	-
Proposed Vedic 8 bit	6.448 ns	90	158
Base 1(8x8)	11.886 ns	-	-
Base 2(8x8)	15.685 ns	-	-
Proposed 16 bit	9.007 ns	452	803
Base (16x16)	15.718 ns	-	-
Base 2 (16x16)	23.064 ns	-	-
	Combinational path delay		
Proposed Vedic 8 bit	13.753 ns	90	158
Base 3(8x8)	13.753	-	-

Table 2: full comparative results

Above it can observe that proposed work has batter results in aspect of area (i.e. less number of Slice) and speed (i.e. logical delay) in 4 bit multiplication as compare to base 3 paper.
Above one can easily observe that proposed work is batter in aspect of speed (i.e. logical delay) in 8 bit as compare to base1, base2 & base3 papers.
Proposed is a design of 4 bit vedic multiplier (our actual research work) and use it to design 16 bit ALU. So one should make comparison with 4 bit vedic only, rest of comparison are also been made

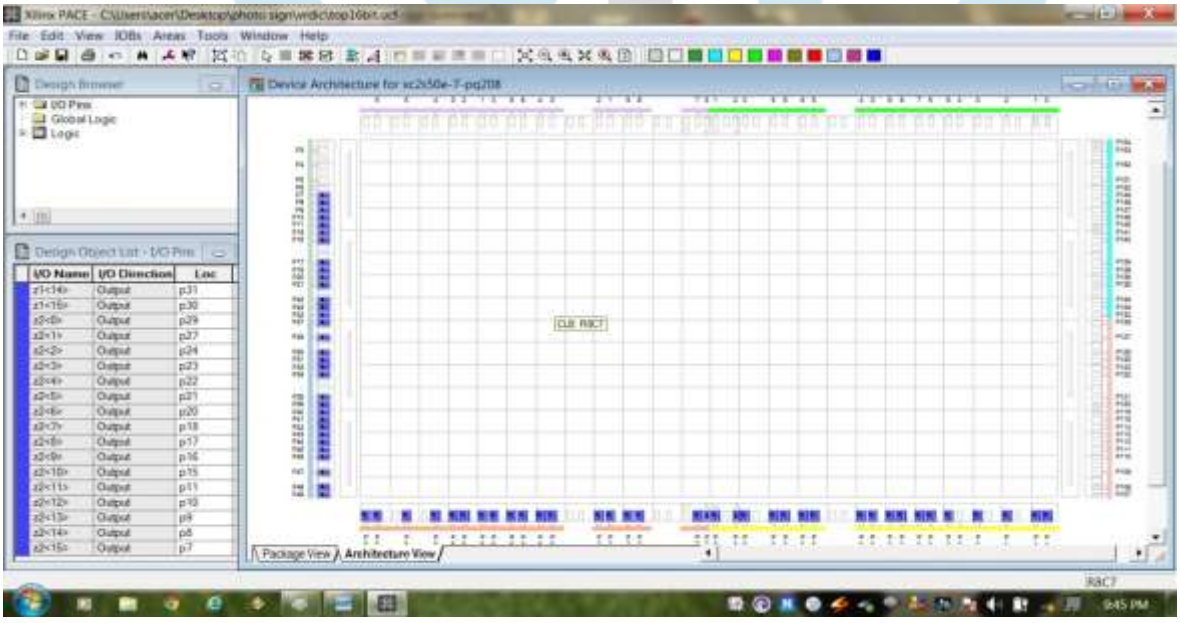

Figure 3 FPGA floor plan of Proposed work

Figure 3 above is the floor plan of proposed work which is designed for generation UCF (user constrain file) for final validation of design on FPGA.

IV.CONCLUSION

Proposed work is designed the 16x16 bit Multiplier and a 16 bit ALU which provides somewhat better results as compare to the available vedic multiplier or all other Multiplier. Proposed design can also be used for optimizing the MAC unit of DSP. And so the optimized designs can be made for FFT, FIR, IIR, and DFT whose performance is dependent on the speed of ALU unit. There are so many application where speed is more concerns than any other things like signal processing in satellite GPS based systems

disaster management system etc. Proposed work give a solution for highly speed ALU and as know ALU is the key element part of software based embedded or general (i.e computer) systems.

REFERENCES

[1] "Lifting Scheme Discrete Wavelet Transform Using Vertical and Crosswise Multipliers", Anthony O"Brien and Richard Conway, ISSC, June 18-19, 2008, Galway,
[2] "Application of Urdhva Sutra", A.P. Nicholas, K.R Williams, J. Pickles, Spiritual Study Group, Roorkee (India), 1984.
[3] 'VLSI Based High Speed Karatsuba Multiplier for Cryptographic Applications Using Vedic Mathematics", Mrs. M. Ramalatha, Prof. D. Sridharan, 2007, IJSCI.
[4] "High Speed Efficient N x N Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Thapliyal H. and Srinivas M.B., 2004, Vol.2, Transactions on Engineering, Computing and Technology,.
[5] Vedic Mathematics, Jagadguru Swami Sri Bharati Krsna Tirthatji Maharaja, Motilal Banarsidass Publication, 1992.
[6] Vedic Maths facts and myths, S.G. Dani, Vol 4/6, January 2001, pp. 20-21, One India One People.
[7] "Vedic Mathematics for Faster Mental Calculations and High Speed VLSI Arithmetic", Himanshu Thapliyal, Invited talk at IEEE Computer Society Student Chapter, Nov 14 2008, University of South Florida, Tampa, FL,.
[8] "Multiplier Design based on Ancient Indian Vedic Mathematics", Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho, Nov. 2008, pp.65-68, International SoC Design Conference,.
[9] Basic VLSI design, PUCKNULL. D.A., and ESIIRAGHIAN, K., Prentice Hall, New Jersey, USA, 1994.
[10] "Vedic Mathematics Based Multiply Accumulate Unit," Devika, K. Sethi and R.Panda, International Conference on Computational Intelligence and Communication Systems, pp.754-757, Nov. 2011CICN 2011.
[11] "The Implementation of Vedic Algorithms in Digital Signal Processing", Purushottam D. Chidgupkar and Mangesh T. Karad, Global J. of Engng. Educ., Vol.8, No.2, 2004, UICEE Published in Australia.
[12] "A Designer"s Guide to Built-In Self-Test", Charles E. Stroud, University of North Carolina at Charlotte, 2002, Kluwer Academic Publishers New York, Boston, Dordrecht, London, Moscow.
[13] www.xilinx.com