PCM MUX Encoder for Telemetry System using VLSI

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Abstract: The progress of highly systematic Very Large Scale Integration (VLSI) technology and instant advancement of FPGA & CPLD architectures has created an uprising in the design approach of complex electronic systems. With highly progressed integrated system design methodology, the discrete event driven system designs are moderately replaced. The present paper illustrates the VLSI based implementation of Pulse Code Modulated (PCM) multiplexer and encoder schemes for telemetry system. It additionally analyses the functional effectiveness as well as performance in the telemetry data acquisition system. The present system accepts slow differing analog Automatic Gain Control (AGC) signals from azimuth elevation tracking error signals as well as telemetry receivers from tracking antenna controller and multiplexes them into single digital Pulse Code Modulated (PCM) stream for real time recording with time stamping on PC based PCM decommuted system. The present system has the potentiality to record this data onto the analog magnetic tape, which can be played back later for review.

Keywords: PCM, MUX, VLSI

1. INTRODUCTION

Any combinational circuit can be represented as multiple inputs with single output. Multiplexers are used to design any digital combinational logic circuit. Hence it is required to design a multiplexer with low power consumption and high speed. The proposed system is a Pulse Code Modulated (PCM) multiplexer cum encoder (PCM MUX Encoder) which accepts slow differing analog AGC signals with maximal bandwidth of l0OHz from azimuth elevation tracking error signals as well as telemetry receivers from antenna controller. Individual signals are then multiplexed into single digital PCM stream for real time recording with time stamping on PC based PCM decommuted systems. PCM is the most broadly accepted form of digital source coding for all types of data and voice signals flexible for transmission over terrene as well as space areas. This is essentially a conventional waveform coding technique, which converts the information into 8 sequence of binary numbers. The PCM MUX-Encoder comprises of an eight channel analog to digital converter (ADC) and CPLD based PCM Encoder. The output of the PCM Encoder goes to analog magnetic tape recorder as well as PC based decommuted system. According to the Nyquist theorem, the sampling frequency (fs) should be at least twice the signal frequency (fm) i.e, (fs>2fm), but in the present case, fs is taken as 5 times fm, for the processing of signal and greater reproduction correspondingly with the Inter Range Instrumentation Group telemetry standard. The input sample is a Pulse Amplitude Modulated (PAM) waveform with samples that appears after every ADC sampling interval. Through the encoder the amplitude of the Pulse modulated signal is then approximated to convert it into PCM signal. The dynamic range covers the minimum to maximum amplitude of (0 to 5) Volts, being split into required number of quantization levels. Each level has been represented by an eight-bit binary code with a dynamic range of 255 levels (2^8 -1). The ADC is having a conversion time of 100 Ms, but in the present design for avoiding the overlapping of two successive conversions additional 60 Ms has been provided. Hence, the total conversion time becomes 160 Ms, which gives sampling frequency of 6.25 kHz. Sampling frequency becomes nearly 780 Hz for each of the eight obtainable analog channels, sampling. The sampling frequency should be 5 times the signal frequency as per the IRIG standard. Thus, the maximum frequency to be sampled becomes 156Hz.

The eight continuous signals are digitized sampled and encoded into 8 bits consecutively by selecting ADC MUX addresses. The 3 bits of address (a, b, c) are generated by a 3 bit write counter for eight channels, which are clocked with a period of 160 Ms. From overcontrolled master crystal oscillator the above clock is generated, which operates at 1 MHz. Using Verilog programming language at RTL code level Other frequencies have been derived from this oscillator frequency. Only after the generation of a valid address, selection of the 1st channel assigned as channel '0' occurs. Address Latch Enable (ALE) signal of pulse width of 2ps is generated in order to meet the timing constraints of the design, after minimum address set-up time (ts) of 50 ns. Then with a minimum pulse width of 2p a Start of Conversion (SOC) pulse is generated. It is observed that with l MHz ADC clock the conversion time of ADC (tec) is 90 Ms approx. Whenever End of Conversion signal from ADC goes high with respect to end of conversion output enable pulse is generated after 50ns to indicate the validity of the converted data. Thereafter, into the internal buffer '0' valid 8-bit data is stored, which is configured inside the CPLD chip. The handshake Signal-timing diagram between the ADC and CPLD is shown in Fig1. Based on the procedure followed for the channel '0' further channel '1' is selected as per the follow-up sequence of the multiplexed ADC channels and eight-bit data is stored in buffer 1. For the rest of the multiplexed analog channels similar procedure is followed. By another independent clock data buffers are read sequentially and with MSB first serially shifted out by 8-bit shift register. Only after shifting all the 8-bit of data of the previous data buffer, Parallel loading of next buffer data into shift register occurs. After the shifting of all eight buffer data corresponding to eight ADC channels two bytes of the

synchronizing patterns (FS1,FS2) are transmitted serially. As per the IRIG telemetry standard byte 'Oxeb' is chosen as FSl and byte '0x90' is chosen for FS2.

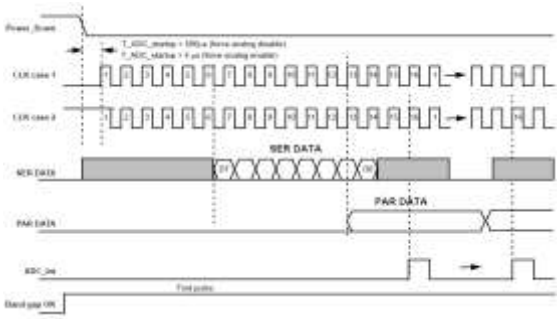

Fig. 1: Timing Diagram of ADC

This is required for post mission analysis on PCM, real time logging and display base-band telemetry system. As long as the global 'reset' pin in the CPLD is high the total sequence repeats continuously. The encoding operation is disabled by active low reset signal. For real time recording onto the magnetic tape recorder TTL signal is converted into bipolar (+5Vor-5V) signal. This helps to playback the recorded data for later analysis. The details of PCM main frame are shown in Fig. 2. The figure shows the mapping of the analog signals to respective ADC channels and posting of corresponding eight-bit digital data over PCM main frame.

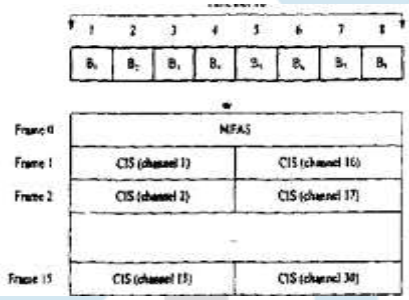

Fig. 2: PCM Main Frame Structure

2. SYSTEM ARCHITECTURE

The block diagram is shown in Fig.3. Various functional blocks used here are

- CPLD chip.
- Voltage Converter.
- ADC (Analog to digital converter).

The ADC 0809 is been used here, this has eight analog input channel out of which any one can be selected at a time for conversion using the address lines (a, b, c) available in the chip. Excluding these, other hand shaking signals are used such as EOC, SOC, OE and ALE. The synchronizer also generates the hand-shaking signal for each channel selection, and waits for the EOC signal from the ADC and initiates a read operation. According to the PCM format a programmable synchronizer block of the CPLD generates addresses. The data read is placed sequentially in an 8-byte buffer and the last 2 bytes are used for the frame synchronizer words. The data from the buffers are put to the output register and read word wise to giving the data out consecutively at a bit rate of 50 kbps. Later, the generated PCM stream's logic level is converted with code converter logic implemented in RTL code within the CPLD.

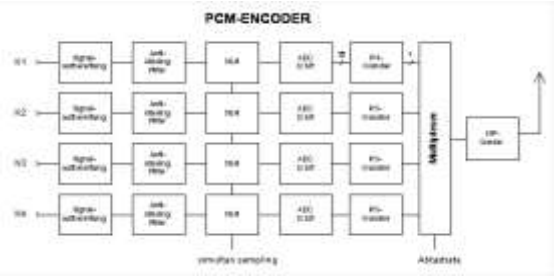

Fig. 3: Block diagram of PCM MUX Encoder

3. DESIGN PHILOSOPHY

Using Verilog hardware description language, the behavioural description of the design is modelled. The program code is synthesized with target device CY37256P154AC in Cypress Warp 6.1 synthesis tool. There are 6 blocks running immediately within CPLD. Block 1 and 4 generate read and write addresses for CPLD and ADC. Blocks 2 and 3 generate control pulses for handshaking between CPLD and DAC and store digitized data from ADC data bus to the data buffer arranged within the CPLD. Block 5 for parallel to serial conversion generates bit address of the shift register. Block 6 is responsible for parallel loading of data from shift register to buffer and make a serial out with MSB first at a programmed bit rate.

4. SYSTEM PEREORMANCE

The design has been verified and configured using CPLD trainer kit, breadboard, and the required hardware components. A sine wave of 100 Hz is given to all the continuous channels and the generated, PCM stream is fed to the PCM decommutated system. All the channels are programmed on thermal chart recorders through the digital to analog converter (DAC). Then with IRIG-B Accumulated Time of the Day (ATD) time stamping data is logged in hard disk of the PC based decommutated system. Time shows satisfactory resu1ts, for different frequencies up to 200 Hz for the graphical plots of some analog channels with respect to ATD.

5. CONCLUSION

In this paper, it has been noted that very steady bit rate for PCM can be obtained with CPLD based implementation. The reduction in complexity of the PCB due to low chip area compared to the digital component based PCM-MUX-Encoder in the old telemetry system. Use of analog multiplexer with high-speed single channel ADC is suggested as a future scope for further number of high frequency analog channels. In the present case, the current design will suffice for exact reproduction of those analog signals as the analog signals are band limited to maximum of 100Hz.

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