Low-Power Ultra-Wideband Low Noise Amplifier Employing Forward Body Bias and Current-Reuse for Wireless Sensor Networks Applications

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***Abstract*: Wireless communication is a critical necessity for biomedical applications, and it has recently sparked a lot of research attention. Low-power receivers are required for such applications, while nevertheless allowing for acceptable communication range and coexistence with other receivers operating in the same frequency band. In wireless sensor network nodes, RF modules account for the majority of power usage. The basis of an RF module is a transceiver. Several methods for lowering the receiver's power consumption have lately been published. The RF local oscillator and RF low noise amplifiers, for example, are the most power-hungry blocks in the whole circuit. The RX power can be greatly decreased to the nanowatt level by using an all-passive RF front-end. We propose to use two stage CS amplifier with a Forward Body Bias (FBB) technique in order to reduce the threshold voltage of MOSFET, and hence, lowering the DC power. We use this method along with the CS–CD current reuse approach. The circuit has two stages: a common-source topology to compensate for the gain of the first stage (M2), and a source-follower (common-drain) topology as a buffer stage to avoid adding a third stage (M3) and improve output return loss. Using this proposed combination approach, we were able to achieve a considerable improvement in the frequency range of 2–11 GHz, according to our experimental results. In a wide frequency range, from 4 to 10 GHz, this improvement includes a lowest noise figure of 2.5 dB, a maximum noise figure of 4.2 dB, and an average noise figure of less than 3 db.**

***Keywords*: Wireless, sensor nodes, Receiver**

1. Introduction

Wireless communication is the transmission of data between two or more sites without the need of an electrical conductor as a transmission medium [1]. Radio waves are used in the most prevalent wireless technology. The intended distances for radio waves can range from a few meters for Bluetooth to millions of kilometres for deep-space radio communications. It includes two-way radios, cellular telephones, personal digital assistants (PDAs), and wireless networking, among other fixed, mobile, and portable applications. Wireless sensor networks (WSNs) are networks of spatially scattered and dedicated sensors that monitor and record environmental variables and send the information to a central point [2]. In data gathering networks, they are in charge of detecting noise, interference, and activity. This enables us to detect relevant quantities, monitor and collect data, create user-friendly displays, and make decisions.

The radio modules in wireless sensor nodes allow them to communicate. If two nodes can send/receive data to/from each other, they are considered directly connected. A sensor communication model (also known as a transmission model) is a mathematical representation of the direct connectivity between sensor nodes [3]. Due to energy limits, WSNs powered by batteries have a limited lifetime. By capturing energy from the environment, energy harvesting technology promises to alleviate the load of replacing or recharging depleted batteries for sensor nodes. Ultra-low power solutions aim to extend the entire sensor network lifetime by reducing energy consumption in the WSN. The limited power consumption resource of the node is the most important factor impacting the possibility of a sensor network malfunction.

In terms of sensor designs, WSNs can have either homogeneous or heterogeneous sensors, with numbers ranging from hundreds to thousands [4]. The communication is primarily done with neighboring nodes using radio frequency electromagnetic pulses. Sensor nodes (SNs) are devices that can detect, decode, and transmit radio frequency data. WSNs are often designed for specialized applications, such as monitoring or tracking, in either indoor or outdoor locations with limited battery power. Several routing techniques have been proposed in recent years to address this issue. Nonetheless, the question of extending the network lifetime in light of sensor capacities remains unresolved.

A WSN system has a large number of nodes that are densely installed either inside or extremely close to the environment. As depicted in Figure 1, each node contains a sensor, an ADC (Analog-to-Digital Converter), an MCU (Micro Controller Unit), a storage unit, a power management unit, and an RF (Radio-Frequency) transceiver. WSN's basic specifications are reliability, precision, flexibility, costs, development difficulty, and power consumption [5]. As all of the nodes are powered by batteries, the most significant WSN specification is power consumption.

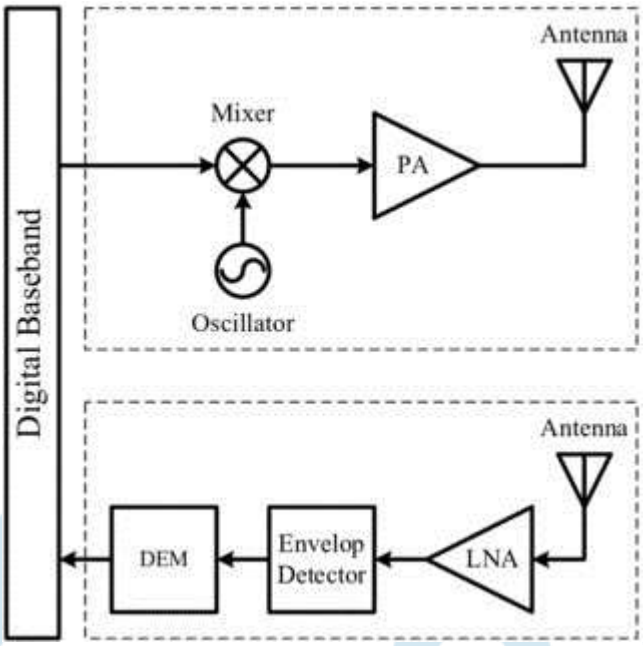

Fig 1: Design of Radio-Frequency Transceiver for WSN

The RF transceiver, which is utilized to realize wireless communication among the nodes, is the most important component of a WSN node. The power consumption of a commonly used commercial chip is unevenly distributed, where TX and RX represent the transceiver's transmitting and receiving modes, respectively. The RF component consumes the greatest power, as can be seen. Aside from that, current RF design encompasses so many topics that IC designers must be well-versed in them. As a result, RF transceiver IC design has emerged as the most difficult research area in the WSN field [6]. Many firms have created highly-integrated chips for RF transceivers as WSN applications grow more common. These chips' shared characteristics can be summarized in numerous ways: 1) a low data rate, 2) high sensitivity, 3) a low power consumption, 4) a relatively low output power, and 5) a simple modulation method are all desirable.

In a WSN, there are numerous approaches of achieving low power consumption: 1) use ad-hoc networks and multi-hop communication to lower radiated power, 2) optimize the trade-off between communication and local computation, 3) build more energy-efficient RF transceivers, and 4) develop more energy-efficient protocols and routing algorithms. In this work, we concentrate more on building a more energy efficient RF transceiver for achieving low power consumption. Although complex schemes such as OFDM (Orthogonal Frequency Division Multiplexing) can be used to maximize spectrum utilization, RF designers prefer simple schemes like OOK (On-Off Keying), UWB (Ultra-Wide Band), FSK (Frequency Shift Keying), BPSK (Binary Phase Shift Keying), MSK (Minimum Shift Keying) and QPSK (Quadrature Phase Shift Keying).

As both modulator and demodulator are straightforward to design, the OOK transceiver can frequently be accomplished with a basic architecture [7]. As a result, the amount of energy used can be lowered. OOK also has the advantage of being able to acquire a high data rate. However, an AGC (Automatic Gain Control) with a wide dynamic range is frequently required; special coding is required to avoid receiver saturation caused by long series of 0 or 1; it is spectrally inefficient; and, because OOK is highly susceptible to interferers, the maximum communication distance of OOK transceivers is usually limited. OOK transceivers can achieve a high data rate, hence some research is focusing on multi-gigabit short-range wireless communications. The transceivers operate at several GHz frequency and consume very little energy per bit.

A signal with a bandwidth more than 500 MHz or a fractional bandwidth greater than 20% is defined as UWB [8]. Despite the fact that UWB is not a modulation scheme, we mention the UWB transceivers separately because the benefits of UWB are significant: Due to the tiny pulse width of a few nanoseconds, it has a high data rate, cheap cost, and low power consumption, and excellent precision in distance measurement. However, there is a severe disadvantage: the spectrum is too vast and the emitting power is limited, resulting in a very small single-hop transmission distance.

FSK transceivers can work without an automatic gain control because only the zero-crossing points of the signal contain relevant information, and additional coding is not required [9]. The modulator and demodulator are both simple to construct. As a result, the FSK transceiver's architecture is basic, resulting in low power consumption and low cost. FSK's spectrum efficiency and ability to avoid interferences are both higher than OOK's, allowing FSK transceivers to communicate over longer distances. Frequency hopping is also possible with FSK systems. FSK transceivers, on the other hand, have a larger complexity than OOK transceivers.

MSK has a higher spectrum efficiency than FSK, but the demodulation is more complicated, and frequency hopping is not possible [10]. These complicated modulations are not suggested for WSN applications with low data rates of many hundreds of Hz. MSK, BPSK, O-QPSK, and even OFDM can be used in a few applications with a high data rate and severe spectrum constraints.

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a low-power signal without lowering the signal-to-noise ratio appreciably. An amplifier boosts the power of both the signal and the noise at its input, but it also introduces some noise [11]. A LNA is usually the initial stage of a receiver front-end, and its main role is to give enough gain to offset the noise of subsequent stages. The sensitivity of the receiver is mostly determined by the LNA noise figure and gain. The RF low-noise amplifier is always followed by a down-conversion mixer. It is one of the most crucial components that is used to convert one frequency to another. In mid-frequency and video amplifiers, ultra-wideband low-noise amplifiers are commonly utilized. Not only is this type of circuit used to magnify video, impulse, and RF signals with bandwidths ranging from DC to several MHz or even tens of MHz, but it is also commonly employed in signal processing.

The major crucial elements in an RF transceiver are a low noise amplifier (LNA) and a power amplifier (PA). A duplexer connects an LNA's receiving path and a PA's broadcast line to the antenna, isolating the two signals and preventing the PA's comparatively powerful output from overloading the sensitive LNA input [12]. There are a variety of LNA topologies aimed towards UWB applications. To achieve appropriate input and output matching, a simplified filter with feedback might be used. Low power consumption can be achieved by using a two-stage common source (CS) with inductive source degeneration and a forward body bias approach. To obtain good gain and minimal power, a two-stage cascade amplifier using resistive feedback and current-reused approaches can be produced.

The precision of signal identification and processing is directly influenced by the performance of the ultra-wideband amplifier circuit. As a result, low-noise, low zero-drift, and ultra-wideband design becomes a critical point with significant engineering and application value [13]. In this work, we propose to use a low-power ultra-wideband low noise amplifier employing Forward Body Bias and Current-reuse that will be suitable for wireless sensor network related applications. Several inconsistencies were successfully resolved with the proposed method, including ultra-wideband and low-noise, high stop-band attenuation and low pass-band fluctuation, high precision gain control and DC zero-drift correction, and so on. Our machine's design has improved characteristics and consistent performance, as well as a higher promotional value.

2. Related Work

This section's goal is to provide a complete overview of the state of the art in implementing circuit with low noise amplifier for wireless sensor network applications. Sohiful Anuar Zainol Murad and others have discussed the topology of a low-power, low-noise amplifier (LNA) for use in wireless sensor networks [14]. The 0.13-m Silterra technology is used to implement the planned ultra-low power 2.4 GHz CMOS LNA architecture. For the first and second stages, the LNA benefits from the forward body bias technique's low power. Two stages are used to improve the gain while keeping the entire circuit's power consumption low. At a low supply voltage of 0.55 V, the total power consumed is only 0.45 mW, according to the results. When compared to other work, the power consumption is reduced by roughly 36%. The input third order intercept point (of -2 dBm) is attained with a gain of 15.1 dB, a noise figure (NF) of 5.9 dB, and a noise figure (NF) of 5.9 dB. The input return loss is -17.6 dB, while the output return loss is -12.3 dB.

Deepak Prasad and colleagues developed a revolutionary low noise amplifier design based on the cascading of common gate, common source, and common drain stages [15]. In the desired frequency band, the cascaded architecture delivers 5–10 dB noise figure and 8.7 dB gain. The input match is provided by the common gate stage, while the output match is obtained by the common drain stage. Here, an input/output match of less than 20 dB/-10 dB is achieved. The reverse isolation is less than 90 decibels. At 7.7 GHz, the 1-dB compression point and third intercept point (IIP3) have been measured to be 27 dBm and 4.3 dBm, respectively. The design is put to the test with a 1 V supply voltage. In 90 nm CMOS technology, the proposed design is implemented utilizing Cadence virtuoso analog and digital design environment.

The battery power will be rapidly depleted due to the increasing processing data rates necessary in applications such as fifth-generation (5G) wireless networks. As a result, unique circuit topologies are required to meet the demand for ultra-low voltage and low power operation. To satisfy the demands of battery-powered communication devices, S. Chrisben Gladson et al presented an LNA operating at ultra-low voltage [16]. When operating at 0.6 V supply, the LNA achieves a high gain (S21) of 18.87 dB, a minimal noise figure (NFmin.) of 2.5 dB in the 3 dB frequency range of 2.3–2.9 GHz, and a third-order intercept point (IIP3) of 7.9 dBm in low-power mode (Mode-I). When operating at 1 V supply, the achieved gain, NF, and IIP3 are 21.36 dB, 2.3 dB, and 13.78dBm, respectively, in high-power mode (Mode-II). The suggested LNA is implemented in a UMC 180 nm CMOS process technology with a 0.40mm2 core area, and the post-layout validation is done with the Cadence SpectreRF circuit simulator.

A WSN is a type of data communication network that consists of a large number of nodes (sensor nodes) that interact via tiny radios over numerous hops (multi-hop) and are equipped with embedded processors, memory, and sensors. For wireless sensor networks (WSN) applications, Ahmad S. Abdullah and colleagues suggested a power-efficient low noise amplifier [17]. The energy consumption of LNAs has a big impact on the design of WSN applications that want to save energy. The transistor (BP1V01M0) is used in this article to get a low noise figure (NF) of 1.2dB and high power gain of 12.63 dB. The design includes a transistor

biasing circuit, a transistor stability test, and the development of a matching network. The simulation results reveal that the suggested LNA design performs at 2.4 GHz with a 2 GHz wideband impedance bandwidth and a 1 mW power consumption.

Meng-Ting Hsu, Kun-Long Wu, and Wen-Chen Chiu studied a low-power CMOS UWB LNA with a cascaded common source and current-reused topology [18]. A systematic strategy is established and explored in depth for the design procedure from narrow band to UWB. Body biased method and current-reused topology can be used to reduce power consumption. The power-constraint noise optimization with inner parasitic capacitance between the gate and source terminal determines the optimum width of the main transistor device M1. The study shows the derivation of the signal amplification S21 using a high frequency tiny signal paradigm. A step-by-step study was used to determine the best design for the entire circuit. The proposed circuit has better S11, gain, noise figure, and power consumption, according to the measurements. With a supply voltage of 1 V, the total power consumption of the proposed circuit, including the output buffer, is 4.6 mW. This work is carried out using a conventional TSMC 0.18 m CMOS process.

Farzaneh Soleymani and colleagues present an area-efficient low-noise amplifier with substantial voltage gain adjustment in the frequency range of 0.3 to 5 GHz [19]. The planned amplifier is made up of two stages of inverter cells, the first of which uses resistance shunt feedback to achieve the desired voltage gain and input impedance matching, and the second of which uses an active floating inductor to extend the circuit's bandwidth. The presented work uses a self-forward-body-bias construction to reduce power consumption and improve overall circuit performance. The suggested circuit has a high voltage gain, low power consumption, a wide frequency range of operation, no physical inductor, and a small occupied active area as a result of these qualities. The amplifier was constructed and simulated in standard 90-nm and 0.18-nm technologies with 0.9- and 1.2-V supply voltages, respectively, with essential 90-nm complementary metal–oxide semiconductor (CMOS) process characteristics described in detail. In 90-nm technology, the developed amplifier consumes 8.8 mW and has a flat variable voltage gain of 22 to 21.2 dB.

Zhiqun Li, Zeng-Qi Wang, and others propose an ultra-low-power common-gate low noise amplifier (CG-LNA) for 2.4 GHz wireless sensor network (WSN) applications [20]. The techniques of current reuse and active gm-boosting are used. The outcomes of the analysis, design approach, and measurement are displayed. On-wafer probing is used to evaluate an implemented prototype utilizing 0.18 m CMOS technology. At 2.44 GHz, measurements show a gain of 14.7 dB and an IIP3 of 2 dBm. At 2.44 GHz, the measured noise figure is 4.8 dB. From 2-3 GHz, S11 is less than -18 dB. From a 1.8 V dc supply, the suggested LNA uses 0.58 mW.

In 0.18m CMOS technology, Roya Jafarnejad et al demonstrated a low power wideband differential Low Noise Amplifier appropriate for multimode receivers and Wireless Sensor Networks [21]. The strict trade-off between input matching and transconductance (gm) is broken by utilizing negative feedback, and the needed transconductance of the input transistor in Common-Gate (CG) LNA is reduced. The present reuse implementation technique considerably reduces power usage. Despite the low PDC, the circuit has a good gain and a low Noise Figure. The LNA construction is completely inductorless, and the core circuit draws only 1.3mW from a 1.8-V supply in a 0.032mm2 space. With a 3dB bandwidth up to 3.3GHz, the maximum voltage gain is 20.1dB. From 20MHz to 3.3GHz, the input matching is better than -16dB. With a third order Input Intercept Point (IIP3) of -2.4dBm, the minimum NF is 3.2dB. This paper presents a 1.3mW differential Common Gate Low Noise Amplifier with no inductor. The concept is to use the tail transistor's transconductance to eliminate the need for a strict trade-off between input matching and power usage. The proposed technique, unlike gm-boosting, does not affect linearity. The circuit is suitable for multimode and Wireless Sensor Network applications because it is low power, low active area, and wideband.

Sensor nodes that monitor critical parameters are connected via wireless medical body-area networks. Because the radio uses a significant percentage of the sensor's energy budget, its power dissipation should be kept to a minimum. The receiver's low-noise amplifier (LNA) is a critical component that must ensure low-noise amplification and impedance matching. Ehsan Kargaran and colleagues have presented an ultra-low-voltage ultra-low-power LNA that has a reduced current consumption of only 160 A and can run with a supply as low as 0.18 V, with the support of transformer-based gate boosting technique [22]. The LNA has a voltage gain of 14 dB, 5.2 dB NF, and 8.6 dBm IIP3 and was created using 40 nm Complementary Metal-Oxide Semiconductor (CMOS) technology. This performance is comparable to that of previous work by the same authors, but with a 4x reduction in the minimum supply voltage.

Emerging health-monitoring applications, including as data transmission through multi-channel neural implants, image and video communication from within the body, and so on, necessitate ultra-low active power (50W), high data-rate, energy-scalable, and highly energy-efficient (pJ/bit) radios. Low average power duty-cycled radios or low power but low-date radios have received a lot of attention in the past. Gregory Chang and colleagues looked into the power-performance trade-offs of each front-end component in a traditional radio, such as active matching, down-conversion, and RF/IF amplification, and prioritized them based on the highest performance/energy measure [23]. The research demonstrates that for a 50W power budget, 50 active matching and RF gain are prohibitive. With OOK modulation, below 50W performance may be achieved up to 10Mbps (5pJ/b) using a mixer-first architecture with an N-path mixer and a self-biased inverter based baseband LNA developed in TSMC 65nm technology.

3. Low Noise Amplifier design

Inductive source degeneration is frequently used in traditional LNA. This structure is notable for providing passive noise matching and better noise performance [24]. However, for operations with a limited power budget, this structure has a low transconductance (gm), which affects noise and gain performance. To help the LNA amplify the signal throughout the target frequency, a band pass filter or Chebychev filter is used in the circuit.

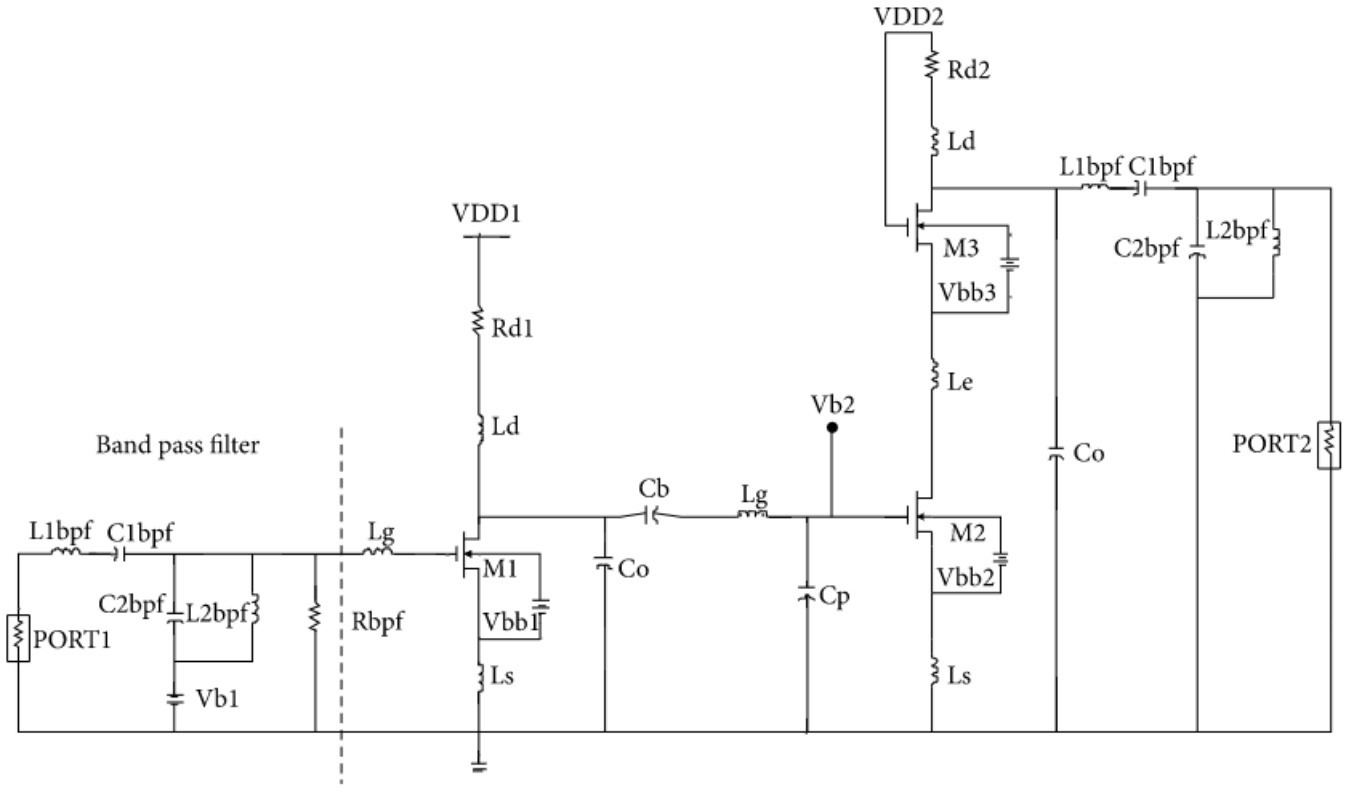

Fig 2: Circuit of the cascade low noise amplifier with band pass filter

The filter's inductors and capacitors are calculated using:

$$L1bpf = \frac{(0.5\ X\ Rbpf)}{\pi(f2C - f1C)} \quad (1)$$

$$C1bpf = \frac{2(f2C - f1C)}{4\ X\ \pi\ X\ Rbpf\ X\ f2C\ X\ f1C} \quad (2)$$

Here f1C represents the lower passband frequency while f2C corresponds to higher passband frequency. To calculate the input impedance of the circuit, we have to use:

$$Zin = S\ X\ (\lg + ls) + \frac{1}{s*cgs} + \frac{gm\ X\ ls}{cgs} \quad (3)$$

The formula is shown to have a significant inaccuracy in both the imaginary and real components. Because the formulas of Zin, Zout, and gain are used to create Lg, Ls, and Ld, the error caused by the formulas causes a significant error in computing the aforementioned elements. As a result, new and accurate calculations are required to reduce error arising. The Chebychev filter's determined values are employed in the circuit's input and output [25]. In other words, the filter used in the circuit's input is the same as the filter used in the circuit's output.

LNA is the first crucial component in the wireless transceiver receiver design. The LNA has a significant impact on signal amplification and ensures that the signal is noise-free. It's a form of amplifier that's utilized in wireless communication systems to boost weak signals recorded by an antenna [26].

Low power consumption can be achieved by using a two-stage common source (CS) with inductive source degeneration and a forward body bias approach [27]. The suggested LNA in this work uses the forward body bias approach and comprises of two common source (CS) stages in a cascade (FBB). FBB is accomplished at each NMOS transistor by connecting it to the bulk of the transistors M1 and M2 via VBULK1 and VBULK2, respectively. The FBB decreased the supply voltage, resulting in lower power consumption. To switch on the device, the FBB approach is utilized to lower the threshold voltage, V TH. As a result, the device

will turn on quickly at 1.0 V, which is a low supply voltage. Transistors M1 and M2 have bulk voltages of 0.7 V and 0.6 V, respectively.

M1 and M2 have 7 m and 10 m finger widths, respectively, and both transistors have a length of 130 nm. In order to achieve a high gain, these values are deemed to have a wider breadth. If the width of M1 is too small, a high value of transconductance gm cannot be obtained, and the bigger bandwidth cannot be achieved. The capacitors C1 and C4 are dc coupling capacitors. The low noise amplifier circuit is represented in figure 3 below.

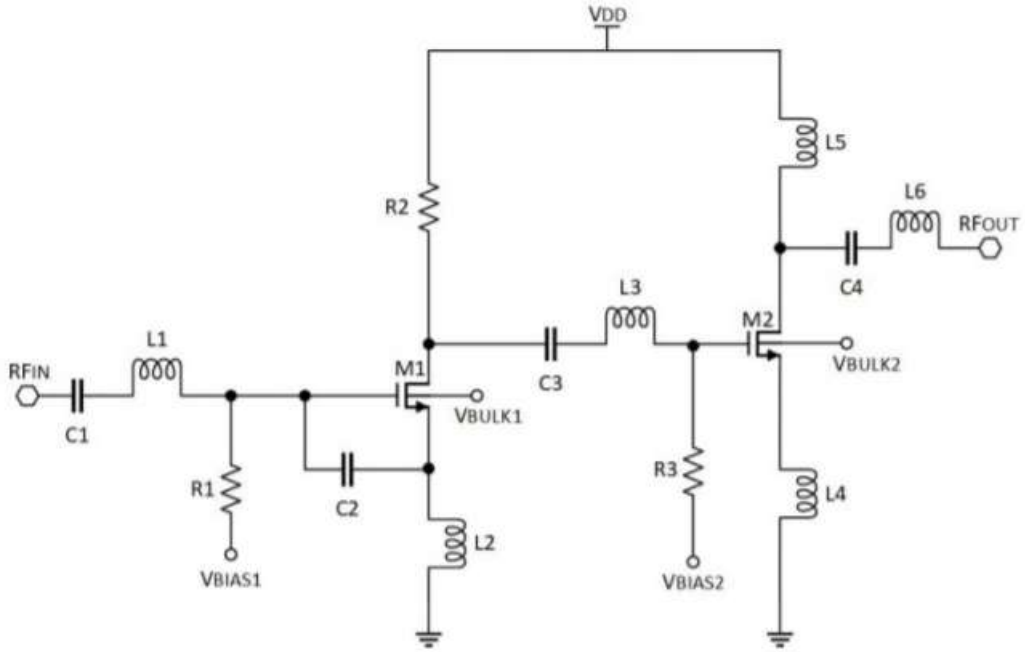

Fig 3: Ultra wideband Low noise amplifier

The L1, L2, and C3 are part of the input matching circuit of the first stage of the UWB LNA, which is matched at 50 input impedance. In order to attain good linearity, the L2 works as a source degenerated inductor. C2 aids in improving the entire circuit's input matching. When M1's width is expanded, the gm increases as well, resulting in a huge parasitic capacitance that limits the bandwidth.

L3 is utilized to extend the bandwidth in order to solve this problem. L5 operates as a shunt peaking inductor in the second stage to compensate for the loss, which can be large in the middle band. L4 operates as a source degenerated inductor, similar to L2 in the input stage, and L5 resonates with C4 to create a flat gain. Meanwhile, the output matching includes the inductor L6. A high gain and low noise figure (NF) UWB LNA can improve the signal-to-noise ratio of a radio frequency (RF) front end receiver. Nonetheless, a number of other requirements must be met, including low power consumption to increase battery life, high gain, strong wideband input/output matching, stability, and linearity, to name a few.

4. Low noise amplifier employing Forward Body Bias and Current-reuse

To minimize reflections between the LNA and the antenna, the input of the LNA must be matched to the output of the filter following the antenna [28]. The conditions are given by:

$$Zsource = Z * in, 1 \qquad (4)$$

$$Zout, 1 = Z * in, 2 \qquad (5)$$

$$Zout, 2 = Z * L \qquad (6)$$

Here Zsource corresponds to impedance seen, (Zin, 1) represents the input impedance of M1, and finally ZL refers to the load impedance. Assuming that Cgd is small, which is usually the case in actual systems, the input impedance of M1 Zin, 1 can be expressed as follows:

$$Zin, 1 = jw0Ls + \frac{1}{jw0cgs} + \frac{gm1}{cgs} Ls \qquad (7)$$

In the above equation, W0 corresponds to the operating frequency. The Zsource is hence the combination of R Source and L source which are obtained as follows:

$$Rsource = \frac{\alpha}{(1-w0C1C2LgRs)+\beta W0} \quad (8)$$

$$Lsource = \frac{-(\beta Rs+\alpha LgC2)}{(1-w0C1C2LgRs)+\beta W0} \quad (9)$$

The final operating frequency can hence be derived as follows:

$$W_0 = \sqrt{\frac{1}{(Lsource+Ls)Cgs}} \quad (10)$$

M1 and M2's separate transconductance are multiplied to get the total effective transconductance. The transistor overdrive voltage has a significant impact on the effective transconductance of the gain stages, as shown by the preceding calculations. As a result, the suggested LNA design uses two cascaded stages to improve the amplifier gain for ultra-low-voltage operation.

The LNA is necessary to provide adequate gain as the first active building block in an RF receiver in order to effectively suppress noise provided by subsequent stages. The overall noise figure in a cascade amplifier can be stated as:

$$F = F1 + \frac{(F2-1)}{G1} + \frac{(F3-1)}{G2G1} + \cdots \quad (11)$$

The noise figure and gain of the n-th stage are denoted as NFn and Gn, respectively. For the total noise figure contribution, the noise figure and gain of the first stage are both critical. As a result, the first stage should be meticulously built to ensure proper input matching and to strike a balance between gain, noise figure, and power consumption.

Rsource could be made closer to Ropt by altering the values of Lg, C1 and C2 for better noise matching, even though Rin, 1 of the MOSFET is smaller than Ropt. However, if Rin, 1 is significantly smaller than Ropt, the C1, C2 (or Lg) value required to bring Rsource closer to Ropt may not be sufficient to fulfill the LNA's input matching requirements. As a result, an inductive source degradation Ls is added. It allows for input matching of up to 50 dB, as well as good linearity and great reverse-isolation, which aids amplifier stability.

Over a UWB frequency range, a current-reuse method lets this silicon CMOS low-noise amplifier achieve high gain and low noise figure with minimal power consumption. When applicable, this file type includes high-resolution graphics and schematics. One amplifying stage is stacked on top of the other using current reuse technology. The cascade arrangement is utilized for LNA, which is appropriate. Higher gain has been achieved without the need of a cascade architecture or an increase in consumption due to the fact that two amplifier stages share the same bias current.

The cascade amplifier (1M and 2M transistors) is the largest contributor to the overall LNA gain since it is essential for the LNA to have high gain and strong circuit stability. The cascade amplifier has a high output impedance and good input to output isolation, in addition to high gain. Drain 1M represents a low impedance point in the cascade amplifier because the drain AC load of transistor 1M is about 1/mg (input impedance of transistor 2M, common gate CG amplifier). Miller gate-drain overlap capacitance can be ignored because the transistor 1M gate to drain gain is modest.

Transistor 4M and resistor refR make up the bias circuit. The biasR resistor is chosen to be large enough to represent high carrier impedance, which prohibits AC signal flow to the bias circuit while also contributing little to total circuit noise. The bias voltage biasV is equal to the transistor's 2M bias voltage. By transferring a signal from the 2M transistor drain to the 3M transistor gate, the large capacitor 1C permits coupling of two amplifier stages. Furthermore, capacitor 2C should be as large as feasible in order to offer the best AC ground for the second amplifier stage. The loads of the first and second amplifier stages are represented by inductors 1L, 2L, and outL as shown in fig 4 below:

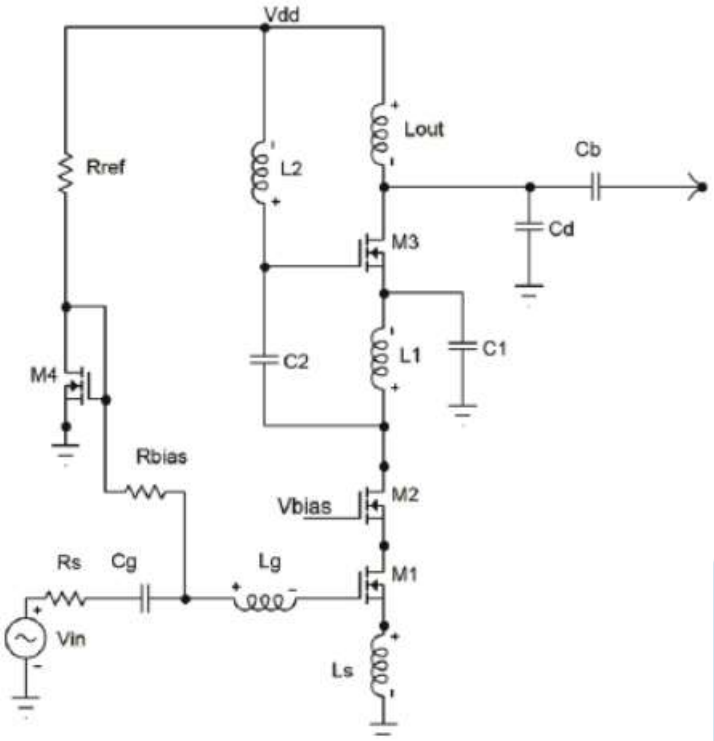

Fig 4: Low noise amplifier with current reuse method

The input and output blocking capacitors gC and bC are used in the described circuit. The total node capacitance at the drain of 3M is parallel to capacitance dC and transformed capacitance bC, as seen in the LNA architecture. This equivalent capacitance creates a parallel resonant circuit with the inductance outL, providing highly desirable band-pass filtering of the output signal as well as increased gain at the centre frequency. The serial resonant circuit's resonant frequency is normally set equal to the output resonant frequency at the LNA input. However, these resonances can be offset from one another if desired, resulting in a lower gain, flatter, and broader response.

The inter stage parasitic capacitance, which is frequently cascaded to the next stage, reduces the bandwidth of the LNA in general. The parasitic gate-source capacitor CGS, for example, bypasses with load RL, reducing bandwidth at 1/RLCGS frequency. To solve this problem, a series inductance L across RL and CGS, which resonates out the CGS, can be used to create a series peaking in frequency response. As more components are introduced into the LNA architecture to achieve desired performance, the power consumption skyrockets and the permitted bias current is limited. As a result, methods that alleviate these issues without degrading LNA performance are sought.

Transistors are typically biased in a weak inversion region, with the bulk of the transistor grounded with the source electrode or linked to a low-level voltage. Although lower current and lower overdrive voltage improve power consumption in some cases, possible drawbacks like as frequency restriction and instability should not be overlooked. Meanwhile, low supply voltage transistors in weak inversion will damage the NF and gain of the LNA, therefore the forward body bias approach with current-reuse arrangement is used to avoid these concerns. The following is the relationship between the threshold voltage Vth and the bulk-source voltage Vbs:

$$Vth = Vtho + \gamma\left(\sqrt{2\Phi f} - Vbs - \sqrt{2\Phi f}\right) \qquad (12)$$

The bulk-source voltage can control the threshold voltage, with the former dropping as the latter increases. The forward-bias positive-negative (PN) junction leakage current from the parasitic substrate-source diode, however, will not be negligible as soon as the bulk-source voltage surpasses a certain value, therefore the threshold voltage cannot be reduced excessively.

When the bulk-source voltage exceeds 0.5 V, the body leakage current grows rapidly, implying that the body leakage current cannot be ignored if the bulk-source voltage exceeds the PN junction turn-on voltage. When the bulk-source voltage Vbs of each transistor is biased at 0.44 V and Vth drops from 0.51 to 0.42 V in this LNA design, the Vgs of each transistor may be lower. Low Vgs, however, will cause transistors to reach a weak inversion area, resulting in significant NF and limiting bandwidth expansion, as mentioned in the previous sections. This is undesirable for a UWB LNA, thus the supply voltage VDD is set to 0.8 V and the gate of transistor M1 is biased with VG1 at 0.57 V. This configuration ensures that the overdrive voltage (Vgs Vth) is not too low and that both transistors (M1 and M2) are in strong inversion operation.

Using the forward body biasing technique, the LNA's supply voltage might be lowered. Not only that, but forward body basing configuration can also modify other performance parameters including as gain, NF, input/output impedance matching, and power dissipation. The bulk transconductance enhancement of M1 and M2 will improve the gain. Meanwhile, if the Vgs is reduced, the induced gate noise, which is inversely proportional to the transistor's transconductance, will be enlarged, especially when the transistors enter the weak inversion region, whereas the NF will be considerably enhanced due to the generated gate noise growth.

Through forward body biasing, a lower supply voltage would improve both gain and NF performance. Furthermore, the cascade LNA's input and output impedances are linked to the gate-source capacitance Cgs of the transistors M1 and M2. Also, the capacitance Cgs is proportional to transistor threshold voltage Vth, and also to the bulk-source voltage, Vbs. In other words, the bulk-source voltage can change the input/output impedance, giving the input/output matching a degree of freedom with the forward body biasing technique.

In the proposed work, all the transistors are adjusted by forward body bias technique for low-voltage and low-power operation without compromising required device characteristics, and transistor M1 in the common-source stage reuses the bleeding current of the CG stage transistor M2 to further reduce the LNA's power consumption. The AC tiny signal is returned by the resistor RF across the gate and drain of M1, resulting in a resistive shunt feedback second-order band-pass filter, which forms the multiple-feedback network with transformer. L3 and L4 finish the inter stage matching. L5 is used as part of the load between M2 and RD to increase gain flatness and eliminate parasitic capacitance in the M2 drain.

5. Results and Discussion

Using design strategies such as current-reuse and taking advantage of modest inversion operation, the proposed circuit proposed in this work has proved the feasibility of an ultra-low power self-oscillating mixer. When we consider the extremely low power consumption, the results are remarkable. Also, in wireless sensor network applications, the suggested SOM's noise figure may match the system requirements; such NF can ensure an adequate sensitivity while maintaining a low data rate, generally 100 kbit/s with a BFSK modulation scheme. The SOM can be paired with an LNA for an extra power usage of 100 W to boost sensitivity even more.

Table 1 shows the performance comparison of different LNA’s proposed in the literature and improvements in our method.

Table 1: Performance comparison of different LNAs

No.	Specification	Inductorless LNA [29]	Feed forward LNA [30]	CMOS cascade [31]	Linear floating-body [32]	Subthreshold LNA [33]	Proposed Method
1	Supply Voltage (V)	1.8	0.8	1.5	1.5	1	1.5
2	Power Consumption (mW)	0.98	0.4	1.5	1.5	0.26	0.25
3	Gain (dB)	16.5	14	13	11	13.6	12.63
4	Noise figure (dB)	2.9	4	2.2	0.95	4.6	1.2
5	Input return loss (dB)	-	-	-11	-33	-10	-44.4
6	Reverse isolation (dB)	-	-	-42.8	-28	-	-18.3

The plot of the supply voltage and power consumption is shown in figure 5 below. The circuit is linear enough to meet the requirements, with an input third order intercept point of -7.5 dBm. The output matching includes the series LC circuits of CL and LL. At a center frequency of 2.4 GHz, both values are tweaked to provide the necessary output matching. R2 and RB are included in the design because they can both boost gain while lowering the output noise figure.

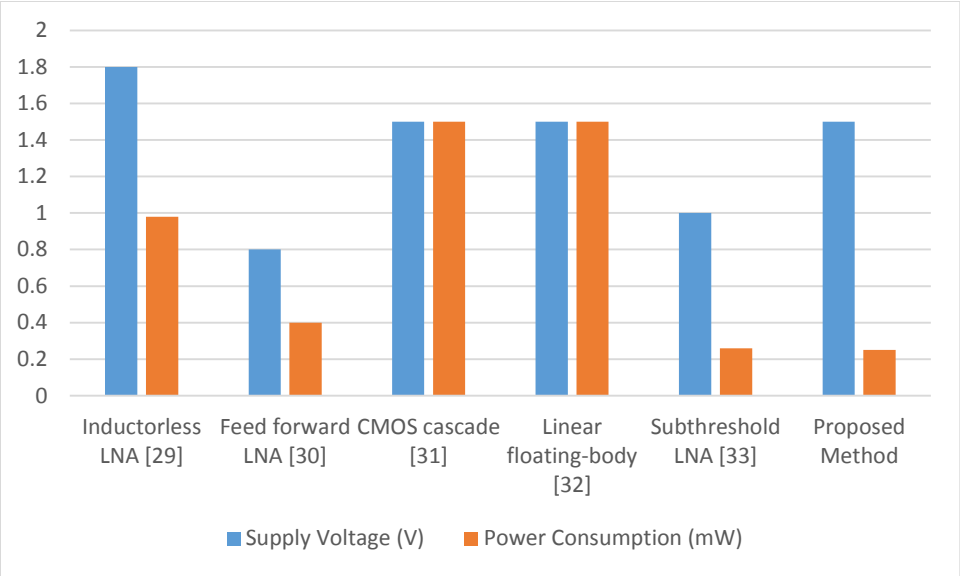

Fig 5: Power consumption comparison across methods

The performance of the proposed circuit is also tested across different voltages as tabulated in table 2 below. The IDC_total, Power, DSB-NF and Gain are all measured for different supply voltages as shown in fig 5.

Table 2: Performance comparison on different voltage conditions

No.	Vdd in mV	350	400	450
1	Idc_Total (uA)	180	243	321
2	Power (uW)	57	100	141
3	DSB-NF (dB)	9.8	7.8	7.9
4	Gain (dB)	28.9	30.4	29.8

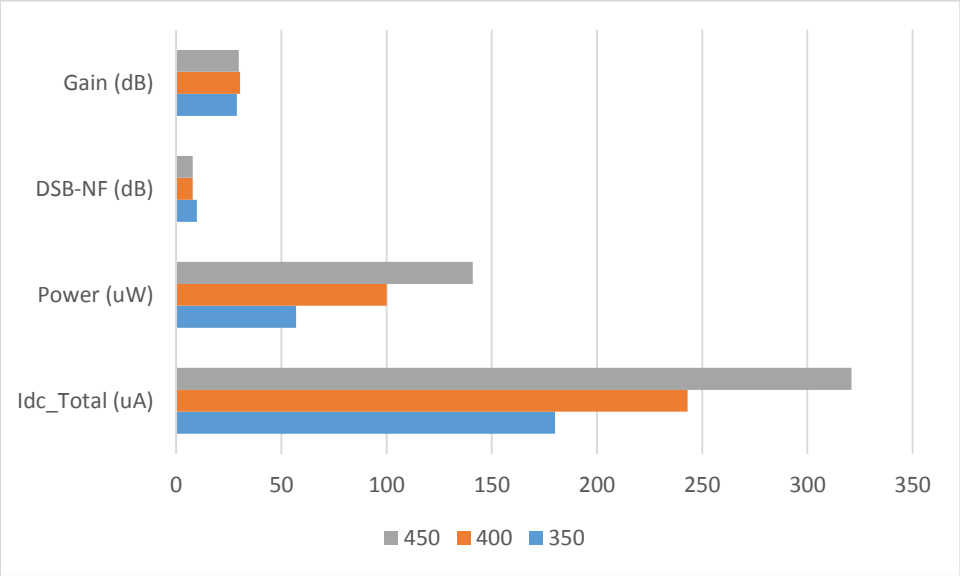

Fig 5: Power consumption across different voltage levels

Conversion gain and noise figure simulations are done while applying a tone at 100 MHz above the operational frequency of 2.4 GHz to test the tolerance to the strongest (-30 dBm) out of band blockers. A 100 MHz offset is applied to the receiver to study noise performance in the presence of blockers. VCO has a varactor for fine tuning and two bits for course tuning. From a 0.4 V supply voltage, it consumes only 100 A. The output waveform of the VCO is presented, and it has a differential peak swing of 200 mV. The VCO can be tweaked between 5.16 and 5.75 GHz. The blocker power in dBm is presented in fig 6 below.

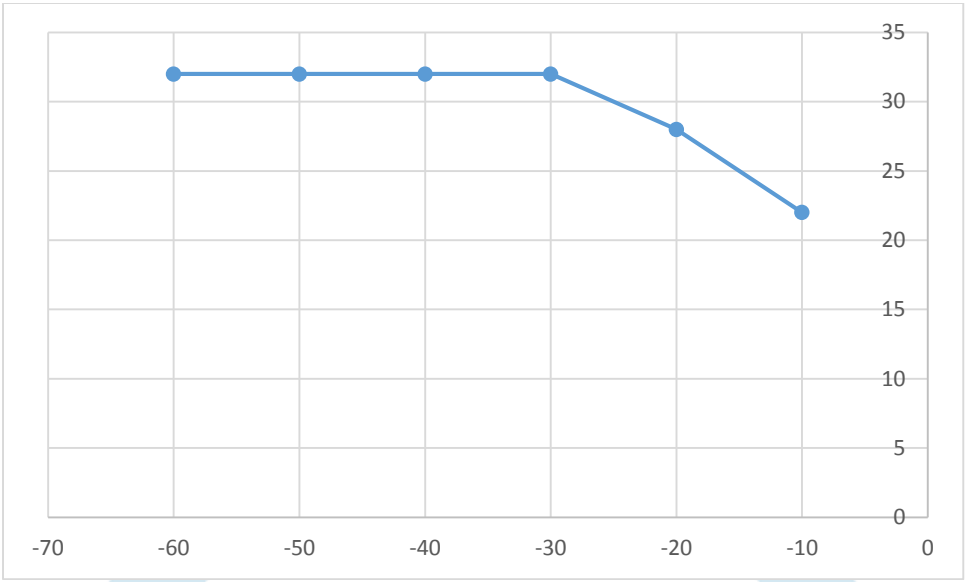

Fig 6: Blocker power measured in dBm

Lower voltage and greater linearity are among the benefits of the proposed ultra-low power circuit. By utilizing an out-of-band RF energy harvesting circuit, the suggested mixer consumes the least amount of power compared to all other recently published studies. The mixer is extremely appealing for WSN applications because of its great linearity and ultra-low power consumption. Fig 6 below shows the conversion gain of the ultra-low power circuit.

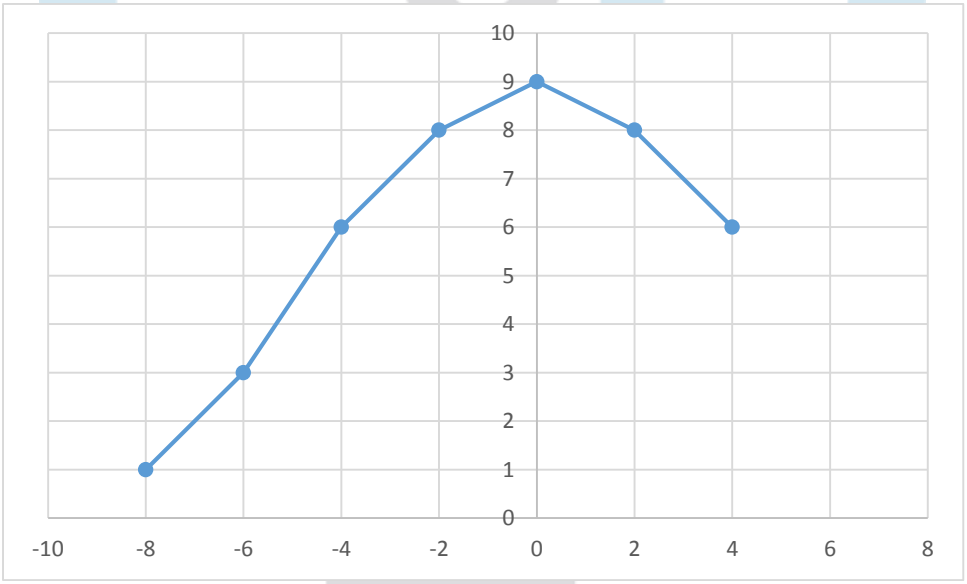

Fig 6: Conversion gain of the ultra-low power circuit

The massive out-of-band RF signals are collected in the out-of-band RF energy harvesting circuit, which is then employed as an AC to DC rectifier. The energy harvesting circuit converts massive out-of-band RF impulses into a DC supply voltage, which serves as a backup power source for the mixer core. The two self-bias currents make use of amplifiers and have a larger transconductance gain, as well as the ability to convert intermediate frequency (IF) voltage signals into currents. The switching step of the mixer core is made up of transistors. At the switching stage, the IF and LO signals are mixed, and the IF signal's spectrum shifting is accomplished. Higher carrier frequencies, on the other hand, provide the main advantages of increased immunity and the ability to integrate antennas, as demonstrated in fig 7.

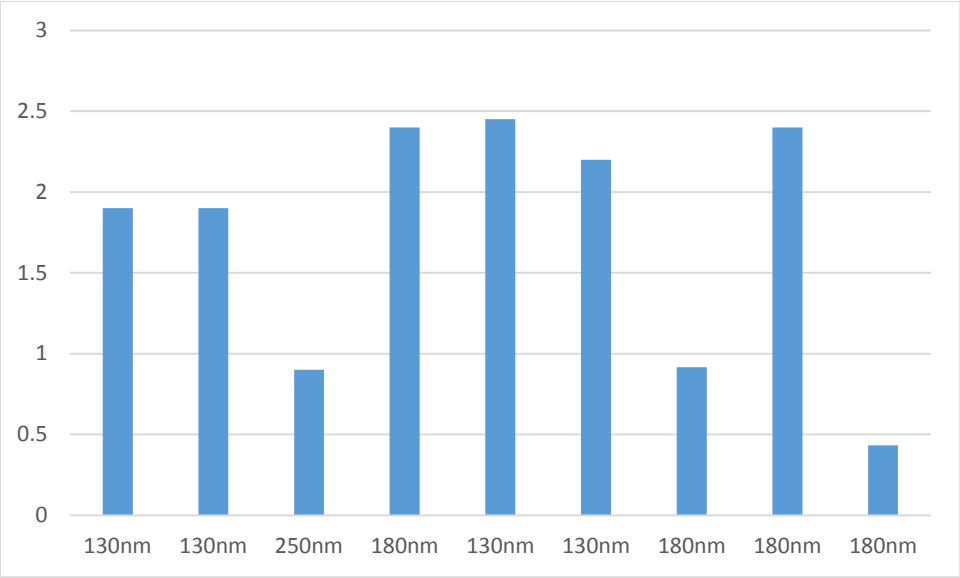

Fig 7: Summary of the reported WSN receivers

In reported WSNs, the transmitter's radiated power is a few milliwatts.

This guarantees that the transmitter's power consumption is in line with the rest of the WSN node's circuits. The power consumption of receiver blocks is estimated to be around 10mW in our research. As a result, we chose 5mW as the transmitter's radiated power, assuming a transmitter efficiency of around 25%. Traditional cellular and WLAN standards place a strong emphasis on spectrally efficient modulation methods like Gaussian Minimum-Shift Keying or Quadrature Amplitude Modulation to overcome band-width restrictions. Furthermore, coherent receivers are required to boost channel capacity for a given bandwidth. However, for sensor network applications, these transceivers require far too much energy.

Based on the simulation results, the performance of this proposed LNA design is comparable to other recently published work. The published works that were chosen are a mix of different technologies and LNA topologies. As can be observed in Table 1, the forward body bias strategy combined with cascade design could result in improved LNA performance. In comparison to earlier work, this work achieved the highest FOM while also consuming less power. The FOM displays the LNA circuit's trade-offs between power consumption, noise figure, and gain. As a result, the comparison is made using the calculated FOM. It is clear from this updated LNA schematic that the LNA's performance has improved when compared to previous efforts.

6. Conclusion

Design methodologies for realizing very low power RF circuits for wireless sensor networks were described in this study. To address these technical constraints of low power consumption, two primary solutions were examined. To begin, the forward bias technique was used, and subthreshold device operation was investigated as a way to reduce power consumption in transceiver circuits. The use of unusually low supply voltages is possible with a forward body biased transistor because its subthreshold voltage can be reduced. In order to capture both RF performance and DC power consumption, a new figure of merit was used to bias RF devices. The design requirement was met using the current-reuse technique. Finally, a mixer and a self-oscillating mixer were built and tested in 130 nm and 65 nm CMOS technologies to show these techniques. Finally, the capacity to construct RF circuits with a nominal power consumption of less than 600 watts was established. For the mixer, the minimal power consumption was less than 400W. The addition of a low noise amplifier to improve the system's sensitivity would be a future improvement. An operational amplifier is required at the high end to provide enough amplification of the baseband signal. The LNA gain must be varied depending on the input signal level to allow the oscillator to work in either a pulling or locking mode while using constant envelope modulation. Future research will focus on the usage of MEMS resonator structures in transceiver circuits, since these components may help to minimize power consumption by eliminating the need for low-Q passives.

References

[1]. M. Challal, A. Azrar, H. Bentarzi, A. Recioui, M. Dehmas and D. Vanhoenacker Janvier, “On Low Noise Amplifier Design for Wireless Communication Systems”, published in the 3rd International Conference on Information and Communication Technologies: From Theory to Applications, 2008.

[2]. Miriam Carlos-Mancilla, Ernesto López-Mellado and Mario Siller, “Wireless Sensor Networks Formation: Approaches and Techniques”, published in the Journal of sensors, 2016.

[3]. Lucia Keleadile Ketshabetswe, Adamu Murtala Zungeru, Mmoloki Mangwala, Joseph M.Chuma and Boyce Sigweni, "Communication protocols for wireless sensor networks: A survey and comparison", published in the journal of Heliyon, Volume 5, 2019.

[4]. M.A. Matin and M.M. Islam, "Overview of Wireless Sensor Network", published in the Wireless Sensor Networks, Technology and Protocols, 2012.

[5]. Antônio Dâmaso, Nelson Rosa and Paulo Maciel, "Reliability of Wireless Sensor Networks", published in the Journal of Sensors, August 2014.

[6]. Amine Didioui, "Energy-aware transceiver for energy harvesting wireless sensor networks", a research article published in the journal of Networking and Internet Architecture [cs.NI], Université of Rennes 1, 2014.

[7]. Michael Kraemer, "Design of a low-power 60 GHz transceiver front-end and behavioural modelling and implementation of its key building blocks in 65 nm CMOS", published in the Micro and nanotechnologies/Microelectronics, INSA de Toulouse, 2010.

[8]. Rashid Saeed, Sabira Khatun, Borhanuddin Mohd Ali, and Mohd Khazani Abduallah, "Ultra Wide Band (UWB) Ad-hoc Networks: Review and Trends", published in the journal of Computer Science, 35-39, 2005.

[9]. Yong Wang, Ranran Zhou, Zhenyue Liu, and Bingbo Yan, "A Low-Power CMOS Wireless Acoustic Sensing Platform for Remote Surveillance Applications", article published in the journal of sensors, January 2020.

[10]. Pere Palà-Schönwälder, Jordi Bonet-Dalmau, Alexis López-Riera, F. Xavier Moncunill-Geniz, Francisco del Águila-López, and Rosa Giralt-Mas, "Superregenerative Reception of Narrowband FSK Modulations", a research article published in the IEEE transactions on circuits and systems, Volume 62, March 2015.

[11]. Ji-Seon Paek, Seung-Chul Lee, Yong-Sik Youn, Dongsu Kim, Jeong-Hyun Choi, Sung-Jun Lee, Junhee Jung and Young-Hwan Choo, "A − 137 dBm/Hz Noise, 82% Efficiency AC-Coupled Hybrid Supply Modulator with Integrated Buck-Boost Converter", published in the IEEE Journal of Solid-State Circuits, September 2016.

[12]. Daniele Montanari, Gerardo Castellano, Ehsan Kargaran, Giacomo Pini, Saheed Tijani, Davide De Caro, Antonio Giuseppe Maria Strollo, Danilo Manstretta and Rinaldo Castello, "An FDD Wireless Diversity Receiver with Transmitter Leakage Cancellation in Transmit and Receive Bands", published in the IEEE Journal of solid state circuits, July 2018.

[13]. Moustapha El Bakkali, Said Elkhaldi, Intissar Hamzi, Abdelhafid Marroun and Naima Amar Touhami, "UWB-MMIC Matrix Distributed Low Noise Amplifier", published in the 14th International Conference on Interdisciplinary in Engineering—INTER-ENG 2020

[14]. Sohiful Anuar Zainol Murad, Anishaziela Azizan, Rohana Sapawi and Tun Zainal Azni Zulkifli, "Ultra-Low Power 0.55 mW 2.4 GHz CMOS Low-Noise Amplifier for Wireless Sensor Network", published in the IETE Journal of Research, November 2019.

[15]. Deepak Prasad, Krishna Datta, Sanjeev Kumar, Partha Paul and Vijay Natha, "A novel design of UWB low noise amplifier for 2–10 GHz wireless sensor applications", published in the Sensors International, 2020.

[16]. S. Chrisben Gladson, Adith Hari Narayana, V. Thenmozhi and M. Bhaskar, "A 219-µW ultra-low power low-noise amplifier for IEEE 802.15.4 based battery powered, portable, wearable IoT applications", published in the Springer journal of SN Applied Sciences, March 2021.

[17]. Ahmad S. Abdullah, Sadeq Adnan Hbeeb, Haidar N. Al-Anbagil, and Abdulghafor A. Abdulhameed, Power Efficient Wideband Power LNA for WSN", published in the 2nd International Scientific Conference of Engineering Sciences, 2020.

[18]. Meng-Ting Hsu, Kun-Long Wu and Wen-Chen Chiu, "Systematic Approaches of UWB Low-Power CMOS LNA with Body Biased Technique", published in the Wireless Engineering and Technology, July 2015.

[19]. Farzaneh Soleymani, Parviz Amiri and Mohammad Hossein Maghami, "A 0.3–5 GHz, low-power, area-efficient, high dynamic range variable gain low-noise amplifier based on tunable active floating inductor technique", article published in the International Journal of Circuit theory and Applications, June 2021.

[20]. Zhiqun Li, Zengqi Wang, Meng Zhang, Liang Chen, Chenjian Wu and Zhigong Wan, "A 2.4 GHz Ultra-Low-Power Current-Reuse CG-LNA With Active Gm -Boosting Technique", published in the IEEE Microwave and Wireless Components Letters, May 2014.

[21]. Sohiful Anuar Zainol Murad, Anishaziela Azizan and Ahmad Fariz Hasan, "Ultra-low power 0.45 mW 2.4 GHz CMOS low noise amplifier for wireless sensor networks using 0.13-nm technology", published in the Bulletin of Electrical Engineering and Informatics, 2020.

[22]. Ali Dehqan, Ehsan Kargaran, Khalil Mafinezhad and Hooman Nabovati, "An ultra-low voltage ultra-low power CMOS UWB LNA using forward body biasing", published in the Midwest Symposium on Circuits and Systems, August 2012.

[23]. Gregory Chang, Shovan Maity, Baibhab Chatterjee and Shreyas Sen, "Design Considerations of a Sub-50 µW Receiver Front-end for Implantable Devices in MedRadio Band", a research article published in the arXiv.org - Networking and Internet Architecture (cs.NI); Signal Processing (eess.SP), 18th October 2017.

[24]. Yang Lu, Kiat Seng Yeo, Alper Cabuk and Jianguo Ma, "A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers", published in the Circuits and Systems I: Regular Papers, IEEE Transactions on 53(8):1683 – 1692, September 2006.

[25]. Yong-Zhong Zhu and Ke Guan, "Design of General Chebyshev Filter for Optimizing the Band-Edge Sensitivity", article published in the International Conference on Communications and Mobile Computing, 2010.

[26]. Ashwini Rajole, "Low Noise Amplifier Design and Analysis for Wireless Voice Transmission", published in the International Journal of Science and Research (IJSR), 2013.

[27]. Jawar Singh and Sunil Pandey, "A 0.6 V, low-power and high-gain ultra-wideband low-noise amplifier with forward-body-bias technique for low-voltage operations", published in the IET Microwaves Antennas & Propagation, January 2015.

[28]. Jong-Gyu Go and Jae-Young Chung, "Active GNSS Antenna Implemented with Two-Stage LNA on High Permittivity Substrate", article published in the Journal of Electrical Engineering and Technology, 2018.

[29] Sobhi J and Koozehkanani ZD, "A sub-mW 2.9-dB noise figure Inductor-less low noise amplifier for wireless sensor network applications", published in the AEU-International Journal of Electronics and Communications, 2018.

[30] Li Z, Huang L and Sun L., "0.4 mW wideband LNA with double g m enhancement and feed-forward noise cancellation", a research article published in the Electronic Letters of wireless communications, February 2014.

[31] Manjula S and Selvathi D, "Design of low power 2.4 GHz CMOS cascode LNA with reduced noise figure for WSN applications", article published in the journal of Wireless personal communications, June 2013.

[32] Madan, A., McPartlin, M. J., Masse, C., Vaillancourt, W., and Cressler, J. D., "A 5GHz 0.95dB NF highly linear cascode floating-body LNA in 180 nm SOI CMOS technology", published in the IEEE Microwave and Wireless Components Letters, 2012.

[33] B. G. Perumana, S. Chakraborty, C.-H. Lee, and J. Laskar, "A fully monolithic 260-µW, 1-GHz subthreshold low noise amplifier," article published in the IEEE Microw. Wireless Compon. Lett., June 2005.