Comparative Analysis and Optimization of Power of SAR based ADC using CMOS 45 nm and 32nm Technology

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***Abstract*: Power and performance are two major issues in design and synthesis of VLSI circuits which depends on different design parameters. In this paper, the design comparative analysis of SAR based CMOS ADC design is performed considering power consumption as a parameter. The simulation results are taken for two different sub-micron technology as 32nm, 45nm with the help of Microwind3.8 EDA simulation tool. The values of model parameters are used from current Berkeley 4 short channel model (BSIM4). We target a resolution of 4-bit using Up-down counter as SAR logic and a power consumption of few milli watts. The SAR ADC is implemented with core VDD as 1.00 V and IO VDD as 1.80V.**

Index Terms: ADC, SAR, CMOS 45nm and 32nm Technology, Low power, Comparative analysis, Low power, comparator, digital-to-analog converter, sample-and-hold

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) translate the analog quantities into digital codes, used in information processing, computing, data transmission and control systems [1] [2]. The requirements on the power consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks [4] [7]. With the same, the trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area. The technology scaling down leads to improved performance. So extra care should be taken while switching from one technology node to others [1] [3] [4].

There is a wide variety of different ADC topologies available [4] [8]. SAR ADCs have a decent conversion speed and overall less chip area in comparison to flash ADCs, and other ADC topologies.

The up-down counter based SAR architecture allows for high-speed, typically low-power ADCs to be packaged in small form factors for today's high demanding VLSI applications.

In a SAR- ADC, internal DAC tries to calculate the value of each sample of the input analog signal through successive approximations and comparisons. Based on the ADC resolution, after a specific number of cycles, the digital word being stored in the successive-approximation register (SAR) corresponds to the analog sample with a specific quantization error [5]. It basically generates one bit per clock cycle, the merits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges. This designed paper presents the comparative analysis for power for ADC designed with 23nm and 45 nm CMOS technology. The main aim to find out and differentiate the effect of design on power consumption using Microwind 3.8 EDA Software tool.

In VLSI designs, more and more complex functions are required in various data processing and telecommunications devices, the need to integrate these functions in a small system/package is also increasing. The levels of integration as measured by the number of logic gates in a monolithic chip has been steadily rising for almost three decades, mainly due to the rapid progress in processing technology and interconnect technology. So we can conclude this change as the logic complexity per chip has been increasing exponentially. This can be proved while dealing with CMOS technologies as 45nm and 32 nm.

II. CMOS 45NM TECHNOLOGY

The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. The default 45 nm technology uses a stack of high K dielectric, metal (TiN) and polysilicon. Some of the key features of the 45 nm technology are given in following table 1 [9] [12] [13].

Table 1: Key features of 45 nm technology

Sr. No.	Parameter	Value
1.	Vdd(V)	0.85- 1.2 V
2.	Effective gate length(nm)	25-40
3.	Ion N(uA/um) for 1V	750-1000
4.	Ion P(uA/um) for 1V	350-530
5.	Equivalent oxide thickness	1.1- 1.5
6.	No. of metal layers	6-10
7.	VTHO	0.240V
8.	TOXE	2.00

III. CMOS 32 NM TECHNOLGY

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area [12] [13]. Due to the advantage and current demand in CMOS technology, the effort has been taken to design proposed SAR based ADC using 32 nm Technology. The main novelties related to the 32 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 32 nm technology is 25nm. Some of the key features of 32 nm technologies from various providers like TSMC, Fujitsu, and Intel are as given below [12] [13].

Table 2. Key Features of 32 nm Technology

Sr. No.	Parameter	Value
1	VDD (V)	0.85-1.2 V.
2	Ioff N (nA/um)	5-100
3	Ioff P (nA/um)	5-100
4	Gate dielectric	SiON, HfO2
5	No. of metal layers	6-10
6.	VTHO	0.250V
7.	TOXE	1.00

Compared to earlier 45 nm technology, 32 nm technologies will offer:

- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

IV. SAR ADC

The SAR-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and logic control unit. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC feedback [1][2][3]. When an input signal is applied to the converter, the comparator simply tells whether the input signal is greater or smaller than the DAC output and gives one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to alter the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. Figure 1 illustrates the conversion procedure of ADC.

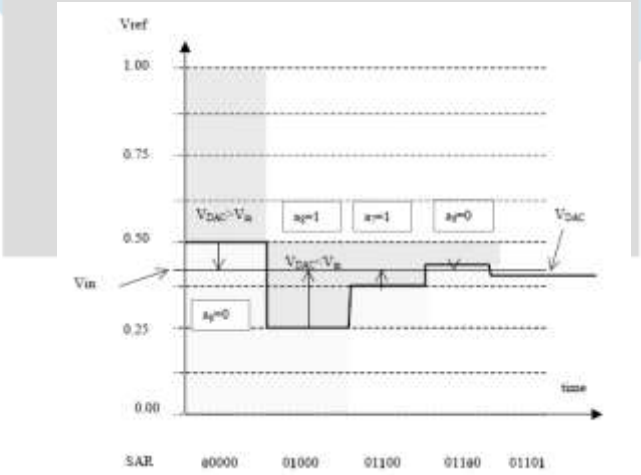

Figure 1: Conversion procedure of ADC

V. ADC DESIGN

The ADC design is basically consists of four subparts as Sample and Hold circuitry, Comparator, Digital to analog converter and SAR register. The functionality is very simple in SAR based ADC. A sample and hold circuit is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time. A sample and hold circuit is to acquire the input voltage (Vin). Sampled signal is than applied to comparators to determine the digital equivalent of the analog signal. It compare the analog signal with another reference signal. Outputs are binary signal based on the comparison. DAC is a function that converts digital data into analog signal. DAC performs inversed function that of ADC. A successive-approximation ADC uses a comparator to successively narrow a range. At each successive step, the converter compares the input voltage to the output of an internal DAC. At each step in this process, the approximation is stored in a SAR. We design the SAR counter logic by simplest method, an Up/down counter to control DAC o/p. It works by starting by binary o/p

8(1000), and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments. We suppose that Vin is a little higher that Vref/2. The SAR counter would increment, else would decrement to get close to Vin value.
After implementing all subparts of ADC as sample and hold circuit, comparator, Up-Down based SAR structure and DAC. We need to insert them all on the single substrate. The Figure 2 shows the physical design of 4 bit CMOS SAR ADC.

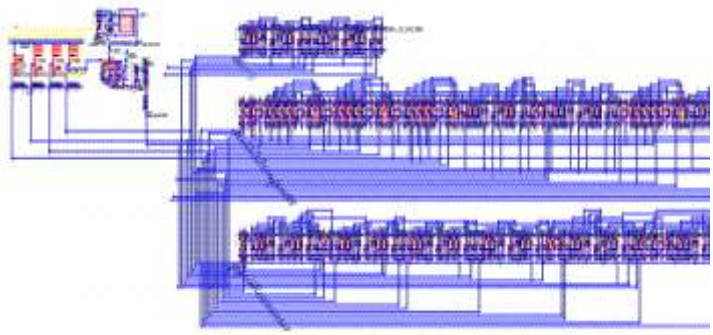

Figure 2: Physical design ADC

VI. SIMULATION RESULT

For ADC design simulation, the input Analog Input as a sine waveform. The main purpose is to find the power value and the behavior of the circuit against the analog or digital signal with specified voltage rages.

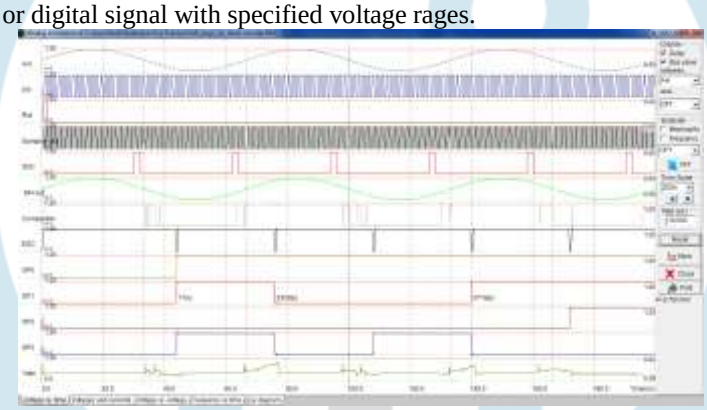

Figure 3: Simulation result of SAR Based DAC

From the simulation graph, we can observe that the conversion starts at the SOC and end s when EOC signal goes high. The conversion follows the digital clock on the data out of the design.

The result are shown in the tabular format in order to find power consumption for standard 45nm and 32nm CMOS technologies.

Table 3: Simulation Result with respect to parameters used

Specification		
Technology Used	45nm	32nm
Architecture	SAR	SAR
Resolution (bits)	4 bits	4 Bits
Core VDD (Volts)	1	1
IO VDD (Volts)	1.8	1.8
Power Consumption (mW)	2.20	1.89
Area	829.6µm2	672.0µm2

VII. CONCLUSION

A physical design of 4-bit successive approximation Register ADC converter suitable for operation at low supply voltage is designed in a standard CMOS 45 nm and 32 nm technology and compared based on the power dissipation. The physical design for various internal parts are designed and combined to form a CMOS based ADC. The Results indicate that the physical design achieves 4-bit conversion and well suited for operation for 1 V in both CMOS 45 nm and 32 nm. The proposed SAR ADC draws a small amount of power 2.20 mW in CMOS 45nm and 1.89 mW I CMOS 32nm which is very less ass compared to the literature data. The area optimization is achieved with the physical area of 829.6µm2 and 672.0µm2 respectively for 45n and 32nm CMOS technology.

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