SEVEN LEVEL MULTILEVEL INVERTER WITH REDUCED SWITCHES USING NOVEL DESIGN

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***Abstract*: The Multilevel inverter usage has been expanded since the last 10 years. These new sorts of inverters are appropriate in different high power and high voltage applications because of their capacity to orchestrate waveforms with improved yield. This venture presents equipment seven level staggered inverter, utilizing microcontroller-based equipment. The staggered inverters certainly stand out enough to be noticed because of the particularity and effortlessness of control. The advancement of high-voltage semiconductors to drive inverter frameworks proceeds. According to a pragmatic perspective, staggered inverters can be founded on reasonable arrangements for applications where a high result voltage can be created utilizing medium voltage gadgets. Notwithstanding this central trademark, staggered inverters have top-notch execution because of the age of a ventured yield voltage nearer to the sine waveform which decreases the sounds in the result waveform**

***Index Terms*: MLI-multi level inverter; Microcontroller; Octo coupler; Mosfet.**

I. INTRODUCTION

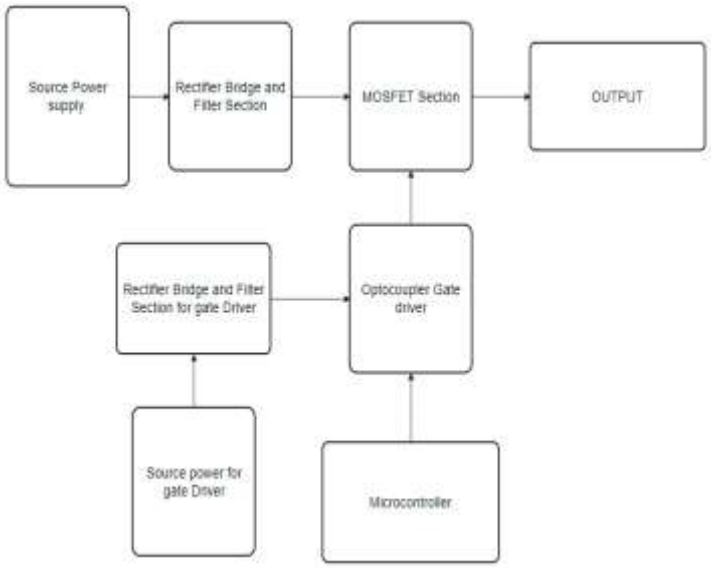
Power gadgets circuits assume crucial part underway of power utilizing environmentally friendly power sources. It is principally used to change over and control the sign. It changes over the sources, possibly it from DC/AC to AC/DC. The AC sources switched over completely to DC source is called rectifier and the DC source changed over completely to AC source is called inverter. The inverter changes over electrical energy. Staggered inverters are applied in space of high-power and medium voltage applications. It delivers an ideal MLI yield voltage from the different DC sources. The staggered inverter focuses because of its benefits in lower exchanging misfortune better electromagnetic similarity, lower music and higher voltage ability. The underlying inverters created were exclusively of two levels. The innovation got progressed and staggered inverters were created which can deliver an ideal result of various voltage levels from many sources of info DC voltage sources.

Staggered Inverter is one of the potential arrangements which is material in numerous applications frameworks. They are able to use in high voltage application with low symphonious additionally and effectively give the require power levels required by the high voltage drives.

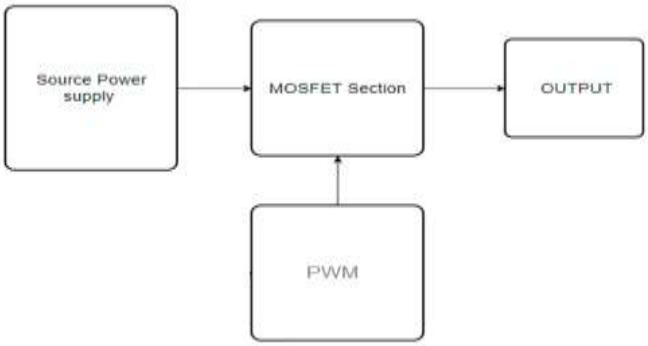
II. METHODOLOGY

The diminished Multilevel inverter likewise makes 7 result levels like the standard H Bridge Multilevel inverter yet purposes 8 switches because of which we can diminish exchanging difficulties. The information voltage divider is made for section input in three branches. Resulting to going between the potential divider the separated voltage occurs after that given to this exchanging area in this way exists make utilizing MOSFETs, along with four diodes. This voltage is next dispatch through the H-development to this result terminal that incorporates four MOSFET. The MOSFET entry will procure influence from PWM block in age and in gear we are including microcontroller and Optocoupler locale for trigger MOSFET.

A. BLOCK DIAGRAM



FIG(a) – BLOCK DIAGRAM ON PROPOSED SYSTEM



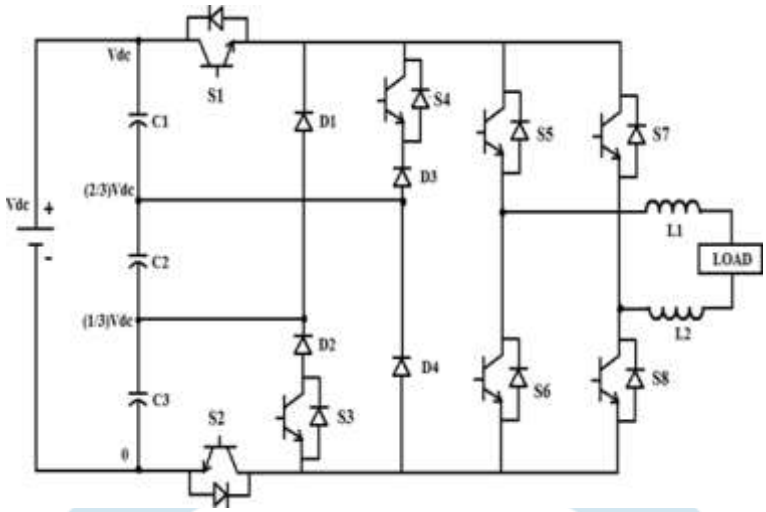
FIG(b) – SIMULATION BLOCK DIAGRAM

The Block outline is rectifier channel circuit. Inverter switches DC over completely to AC. DC source battery is utilized to get steady DC source, yet for this situation consistent DC source is acquired by utilizing rectifier and channel. Rectifier is used for switching AC over completely to DC. To amend both half-patterns of a sine wave, the scaffold rectifier utilizes four diodes, associated together in a "span" setup. The discretionary bending of the transformer is related on one side of the diode length association and the stack on the contrary side. Throbbing DC is sent through channel and unadulterated DC is framed this unadulterated DC is shipped off MOSFET. By this interaction DC is switched over completely to AC this inverter circuit is only enhancer circuit and opto coupler TLP 250.

The microcontroller in the circuit is good for dealing with simply 5v anyway 12v Microcontroller is required, so the microcontroller is set off with PWM to get 12v, this is possible using opto coupler. Aftereffect of the opto coupler is extremely strengthened and sent through MOSFETs or PWM. Optocoupler is used to confine equipment to prevent electrical effect prospects or to bar unfortunate uproars. The diminished switch MLI furthermore makes seven outcome levels like standard H Bridge Multilevel inverter yet purposes 8 switches in light of which we can decrease trading hardships. The information voltage separator consists of 3 capacitors related in cascaded named C1, C2, & C3. Coming about to going across voltage separation the disengaged voltage then transferred to the H-range that is made utilizing Four diodes and MOSFETs. This voltage is next dispatch through H-stage to this result terminal that contains 4 MOSFET and from this the result will be seven level.

B. **REDUCED SWITCH MLI**

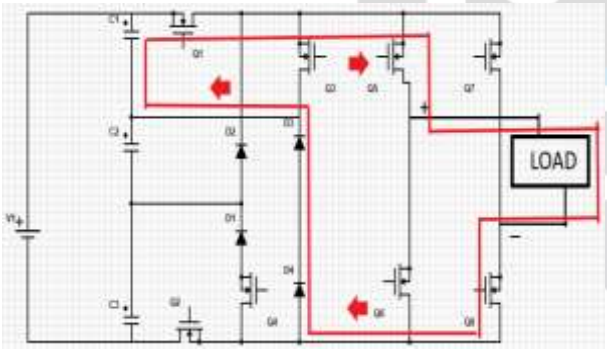
The diminished switch Multilevel inverter comparatively makes seven result levels like normal H Bridge Multilevel inverter yet purposes eight switches due to this it can diminish exchanging difficulties. The below figure displays circuit of Multilevel inverter. This information voltage separator consists of 3 capacitors with cascade connection of C1, C2, and C3. Resulting to next dispatch through voltage separator this distributed is next dispatched through the H-length that is consisting of four diodes and MOSFETs. The voltage is transferred through H-extension to this result end that incorporates 4 MOSFET.



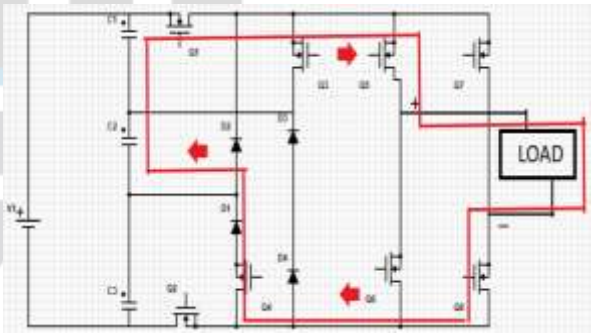
FIG(c) -- CIRCUIT REPRESENTATION OF MLI OF SEVEN LEVEL WITH DIMINISHED SWITCHING CONFIGURATION.

C. OPERATION METHODLOGY

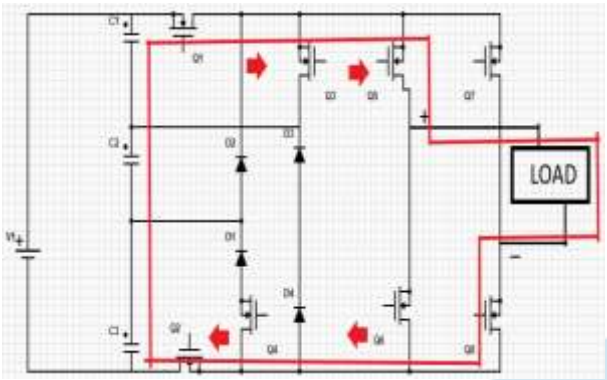
- Considering the information voltage (Vi), the seven levels acquired are: 0, ⅓ Vi, ⅔ Vi, Vi, - ⅓ Vi, - ⅔ Vi and - Vi. This turning out standard inasmuch as every voltage level is as per the going with, this displayed in below fig (3).
- Considering outcome voltage level (Vo = ⅓ Vi), for the positive half cycle switch Q1 is turned on. Q5 & Q8 switches are moreover turned on & this energy is contributed by C1 Capacitor for instance (⅓ Vi).
- Considering outcome voltage level (Vo = ⅔Vi), Q1 & Q4 switches are turned on. This Q5 & Q8 switches too turned on & this energy is contributed by C1 & C2 capacitor for instance (⅔Vi).
- Considering outcome voltage level (Vo = Vi), Q1 & Q2 switches are turned on. This switches Q5 & Q8 too turned on & this energy is contributed by capacitor C1, C2 & C3 (Vi).
- Considering outcome voltage level (Vo = - ⅓ Vi), for the negative half cycle switch Q2 is turned on. This Q6 & Q7 switches are in like manner turned on & this energy is contributed by C3 capacitor for instance - ⅓Vi
- Considering outcome voltage level (Vo = - ⅔Vi), Q2 & Q3 switches are turned on. This Q6 & Q7 switches too turned on & this energy is contributed by C3 & C2 capacitor (- ⅔Vi).
- Considering outcome voltage level (Vo = - Vi), Q2 & Q1 switches are turned on. This Q6 & Q7 switches too turned on & this energy is contributed by capacitor C1, C2 & C3 (- Vi).
- Considering outcome voltage level (Vo = 0), Q5 & Q7 switches are turned on.



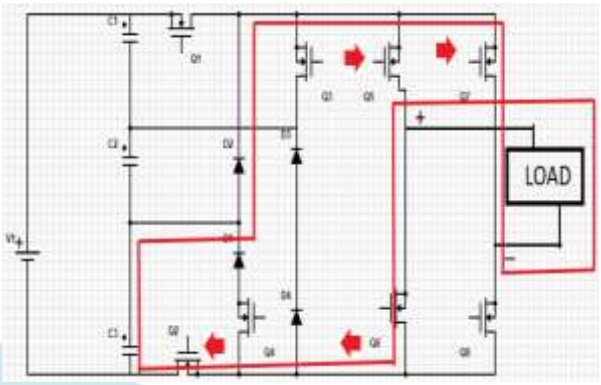
(A)



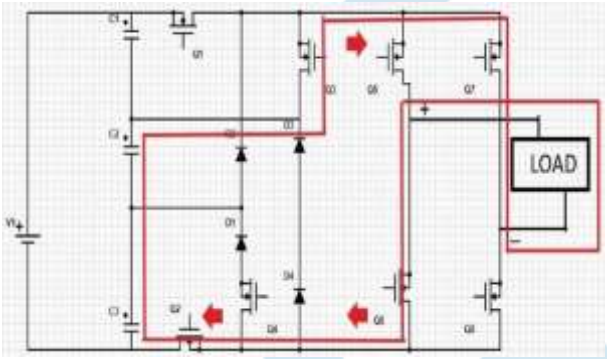
(B)



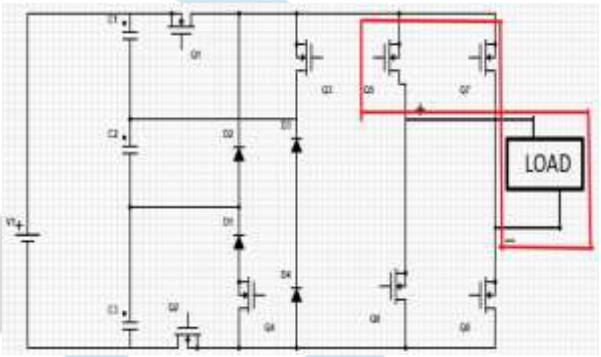
(C)



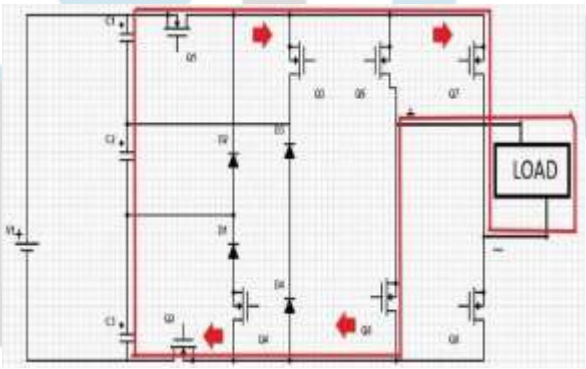
(D)



(E)



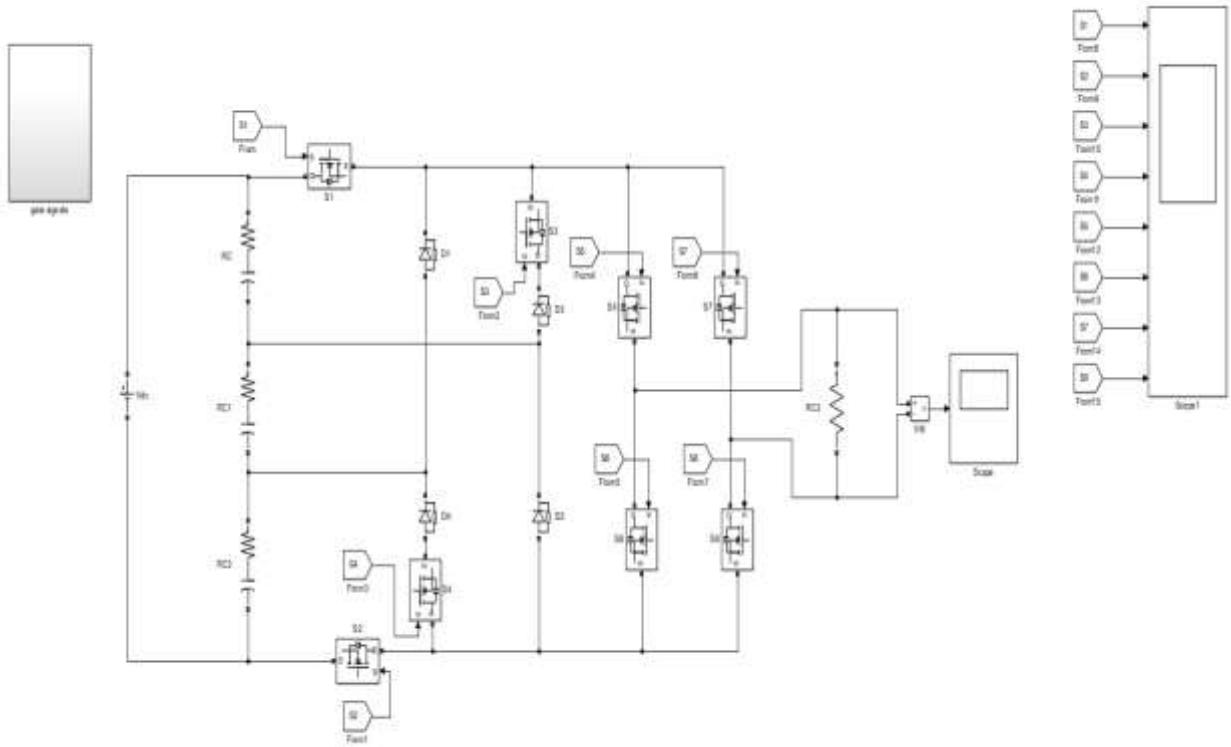
(F)



(G)

FIG(d): FLOW OF CURRENT & POSITION OF SWITCHES- (A) +1/3 Vi, (B) +2/3 Vi, (C) Vi (D) -1/3 Vi, (E) -2/3 Vi (F) -Vi (G) 0

III. SIMULATION RESULTS



FIG(e) – SIMULATION VIEW

The Proposed 7 level inverter is simulated using matlab Simulink. Fig (6) and (7) shows the output voltage and current of proposed seven level inverter with reduces switches using Pulse width modulation

	0	1	2	3	2	1	0	-1	-2	-3	-2
S1	0	1	1	1	1	1	0	0	0	1	0
S2	0	0	0	1	0	0	0	1	1	1	1
S3	0	0	0	0	0	0	0	0	1	0	1
S4	0	0	1	0	1	0	0	0	0	0	0
S5	1	1	1	1	1	1	1	0	0	0	0
S6	1	0	0	0	0	0	0	1	1	1	1
S7	0	0	0	0	0	0	1	1	1	1	1
S8	0	1	1	1	1	1	0	0	0	0	0

TABLE 1. REDUCED SWITCH MLI SWITCHING TABLE

50 Hz time is 1 sec as per 50HZ required

Total Switching sequence 12

1 cycle time

= 1 sec / 50

= 20 mili second

20 mili sec to micro sec
= 20000

So Total delay in one cycle is 20000 micro second
In each switching time required

20000/ 12

= 1666 Time delay

Time period = 1/f = 1/50 = 0.02
Pulse width = Switch ON position / Total no. of modes * 100
Phase delay = Total Time period / Total no. of modes * mode number

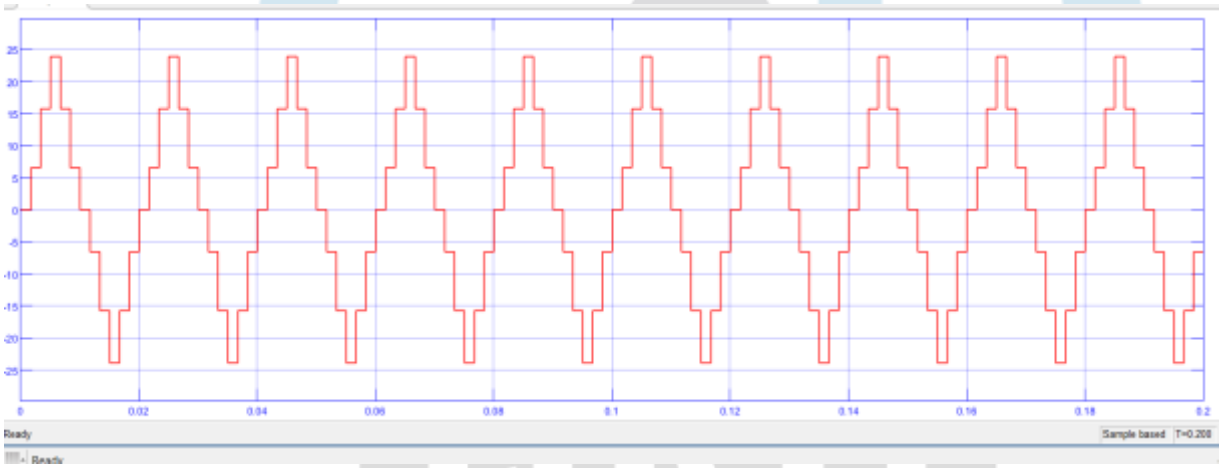


FIG (f) -- OUTPUT WAVEFORM

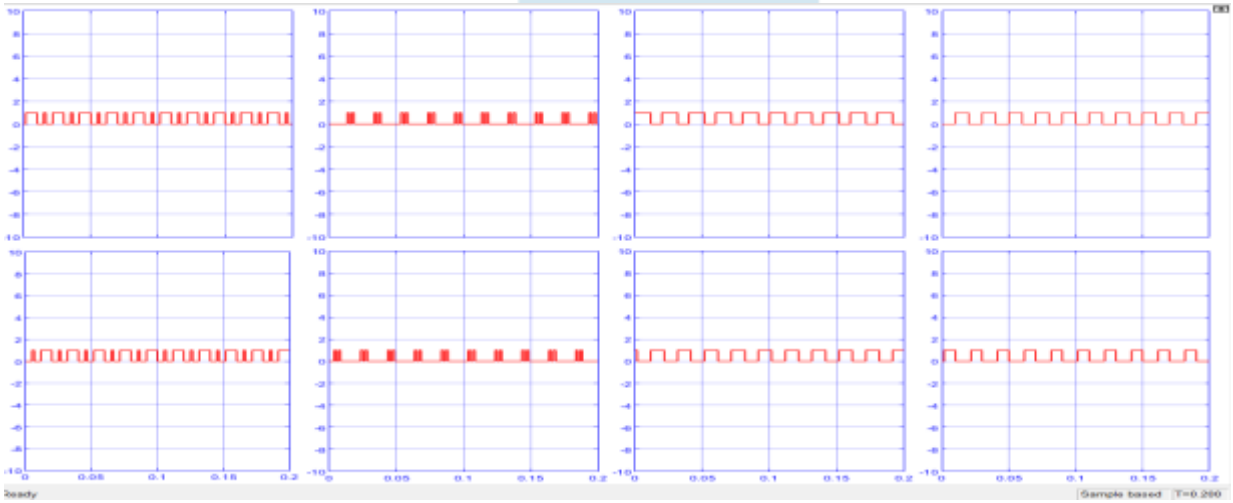


FIG (g) -- WAVEFORM OF PWM FOR ALL GATES

IV. FUTURE SCOPE

This execution is a finished answer for staggered inverter. In this Implementation in future, we likewise can carry out Hardware with various source power moreover. In this plan we are utilizing one information power source. In future likewise we can execute for crossover framework. in future this execution will increment as we are carrying out this with advance way.

V. CONCLUSION

A staggered inverter is utilized in power change technique for, high power applications and high voltage an option for now, transportation frameworks, transmission framework and modern work drives and so on. Staggered inverters are hence observed to be entirely reasonable for the voltage drive activity. More significant level inverters give better execution when contrasted with lower-level inverters. Equipment we executed with atmega328 microcontroller. The result waveform tried in CRO in equipment project. Reenactment we are carrying out utilizing MATLAB reproduction instrument.

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