DESIGN OF THREE-STAGE COMPARATOR AND ITS MODIFIED VERSION USING LECTOR TECHNIQUE

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ABSTRACT---This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by canceling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the conventional two-stage and the proposed three-stage comparators are implemented in the same 45nmCMOS process.

INTRODUCTION

Many applications nowadays, such as signal filtering and processing, are done digitally. Designers of digital integrated circuits (IC) must create a fast analogue to digital converter (ADC) circuit because the ADC affects the applications' overall performance. Power consumption and processing time are crucial in these applications. A comparator is one of the most common building pieces of ADCs. As a result, the comparator needs to be fast and efficient. A comparator compares two analogue signals and produces a binary signal as a result of the comparison. The comparator requires a preamplifier circuit since the input signals are often of low amplitude. The benefit of the differential amplifier will be quite high. It amplifies the difference in voltage between inputs.The decision-making circuit or latch is connected to the preamplifier's output. By comparing the signals, the decision-making circuit determines which is greater. Preamplifier-based comparators are typically used in flash and pipeline ADC architectures. A regenerative comparator with a back-to-back latch degree and high quality remarks is a preamplifier-primarily based comparator. To lessen the kickback impact, a comparator with a latch uses a preamplifier. This will aid in noise discount.
The memory unit that saves a energy on the gate of an inverter is known as a latch. A dynamic latch is popular analogue circuit architecture because it offers good speed and accuracy. Using a cross-coupled pair of PMOS and NMOS transistors, a dynamic latch circuit can be created. The latch is divided into two phases, each of which is controlled by a clock (CLK) level that is either low or high.

LITERATURE REVIEW

Babayan-Mashhadi, S., &Lotfi, R. Analysis and Design of a Low-Voltage Low-Power Double Comparator. in which a fashionable double comparator's circuit is tweaked for less-energy and fast performance even at low deliver voltages. The superb comments all through regeneration is strengthened with out changing the layout and via way of means of including some transistors, ensuing in a appreciably shorter put off time and decrease energy intake [1]. Khorami, A., &Sharifkhani, M. High-velocity low-energy comparator for analog to virtual converters. A two-level dynamic comparator with low energy and rapid velocity is validated. To decrease the primary level's energy in take, The voltage swing issue additionally offers a robust power for the second one level all through the evaluation segment, growing the assessment velocity[2]. NeethuPrakash, SAR ADC Using Low Power Comparator for Precise Applications. The proposed comparator is an superb desire for excessive-velocity, low-energy packages. The energy intake is substantially decreased while the preamplifier is grew to become off after the premiereput off. As a result, it lowers energy in take even as growing velocity [3]. Lu, J., & Holleman, J. A Less-Power more-Precision Comparator With Time Domain Bulk Cancellation. To reduce input-referred offset of a low-energy excessive-precision dynamic comparator with little extra energy intake and put off, a completely unique time-area bulk offset cancellation approach is implemented. With a massive variety of not unusual place mode input, the offset cancellation technique can offer short and strong convergence without introducing detectable offset or noise[4].

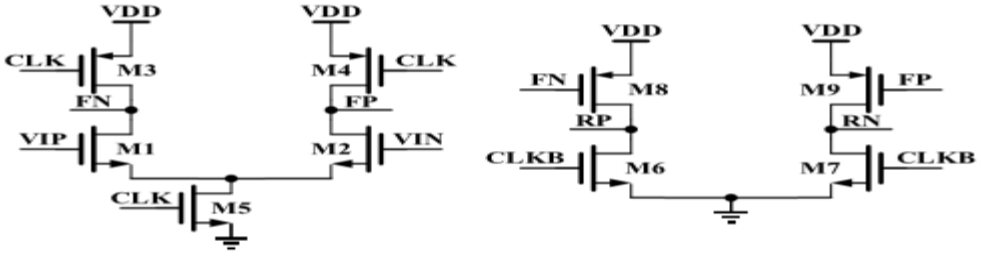
EXISTING METHOD

Excessive-speed analog to-digital converters (ADCs) digitize the signal on the front-give up acquire channels in modem verbal exchange structures as the link among digital processors and the analogue global. As a end result, the conversion speed and precision of ADCs are decided with the aid of the overall performance of comparators. A digital latch circuit with an infinite advantage, pre amplifier makes up a super latched comparator. Comparators can combine high-quality feedback to acquire almost unlimited advantage due to the fact the amplifiers employed in them do no longer need to be linear or closed-loop. Due to less gain in the implementation of the preamplifier layout, the real latched comparators use a finite benefit amplifier circuit and a advantageous remarks dynamic latched circuit. A latched comparator's operation may be damaged into tiers because of its precise architecture: monitoring and latching. The following dynamic latch circuit is grew to become off inside the monitoring level, and the preamplifier amplifies the input analogue differential voltages. The instant currents of transistors are associated with the inputs of the comparators via parasitic gate-supply and gate-drain capacitances, rendering the disturbances undesirable. It is a phenomenon known as "kickback noise have an impact on." The mixture of adjustments from regeneration nodes in flash ADCs wherein a excessive wide variety of comparators are became on or off at the identical time would possibly come to be enormously great, resulting in wrong quantization code output. However, to lower the offset voltage, these solutions require a high voltage gain, which loses effectiveness when the drain resistance decreases owing to technology scaling. Furthermore, achieving a broad bandwidth amplifier necessitates a high power consumption amplifier. A dynamic comparator with an offset compensation function, on the other hand, was presented. On this method, every comparator's input sign is brought in flash type ADC because the reference voltage, and the weight capacitances of the comparator's output node are digitally regulated so that the comparator's output reaches the suitable fee. But, as the ADC's resolution is improved, the calibration time increases dramatically.

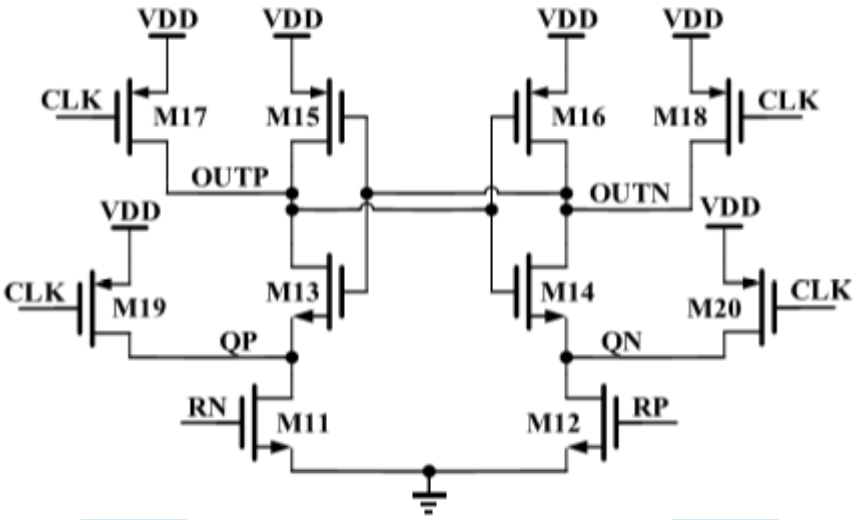
PROPOSED METHOD

Ultra Wide-Band and Wireless Personal Area Network virtual Wi-Fi verbal exchange packages require low-strength, excessive-pace ADC's to transform radio frequency/intermediate frequency alerts into virtual shape for baseband processing. In ADC, a comparator is an essential tool this is typically applied. ADC's, records transfer, switching strength regulators, and quite a few different packages all employ comparators. In excessive-pace ADC's, the comparator layout is important. In comparator layout, strength intake and pace are important factors. The comparator is a critical constructing block for all excessive pace ADC's, unbiased of architecture, and it influences the general overall performance of records converters to a wonderful extent. It carries records which include the most sampling rate, a chunk resolution, and standard strength intake. Comparators are perhaps the maximum underappreciated and underused monolithic linear component. This is regrettable due to the fact comparators are some of the maximum adaptable and extensively used additives available. The IC op amp, whose adaptability lets in it to dominate the analogue layout arena, is in charge for a huge a part of the shortage of awareness. Comparators are normally notion of as 1-bit A/D converters that poorly specific analogue records in virtual shape. In a strict sense, this factor of view is correct. It additionally has a wastefully restrictive viewpoint. Comparators do not "without a doubt compare, "simply as op amps do not "simply amplify." Comparators, especially excessive pace comparators, may be applied to assemble linear circuit capabilities as state-of-the-art as any op amp-primarily based totally circuit. Getting excessive overall performance effects calls for really appropriate use of a quick comparator and op amps. Op-amp primarily based totally circuits, in general, employ their cap potential to exactly near a remarks loop. In a super world, such loops might be maintained indefinitely. Comparator circuits, on the opposite hand, are often depending on pace and function a time-various output. While every approach has advantages, combining the 2 produces the best circuits. Figure four depicts the 3-level comparator.The pre dominant alternate from the Miyazawa comparator is the addition of a 2nd preamplifier (the second one level). This greater preamplifier serves as an inverter; permitting the latch stage to use the nMOS input pair M11–12 in place of the pMOS enters pair, ensuing in quicker processing. The extra preamplifier more over provides voltage advantage, growing regeneration pace and reducing enter referred offset and noise. Despite the fact that the second one preamplifier accelerates the process, it moreover affords to the eliminate due to the fact the amplified signal have to by means of pass thrutiers rather than one in advance than attaining the latch level. As a result, it's miles crucial to speak about whether or no longer the benefit of the extra do away with outweighs the disadvantage. These consequences in a large gate–deliver voltage identical to VDD for the second one-degree enter pair M8–nine. As a end result, M8–9 has sufficient contemporary to hastily pull up RP and RN. This shows that the second one level's extra put off is minor (about 20 play station in publish-format simulation) in comparison to the latch stage's large take away (approximately2 hundred play station in publish-layout simulation).

This is understandable for the cause that the second one level is a dynamic inverter with little put off. The three-level comparator's first-level output load (M8–9 in Fig. 3) is most effective M8–nine.The output load is reduced with the resource of the use of numerous instances, improving the amplification pace.

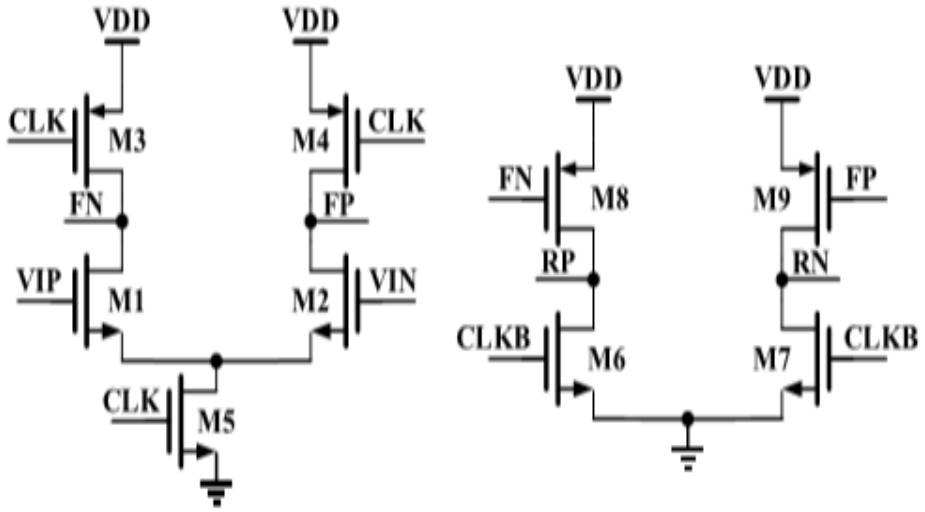


(a)



(b)

Fig.Three-stage comparator (a) First two stages (preamplifiers). (b) Third stage (latch stage).



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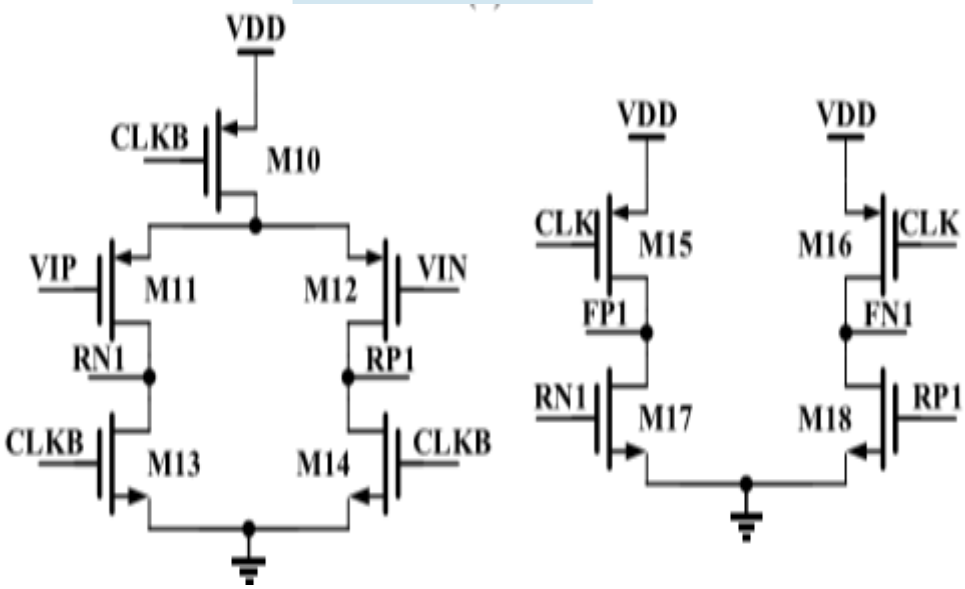

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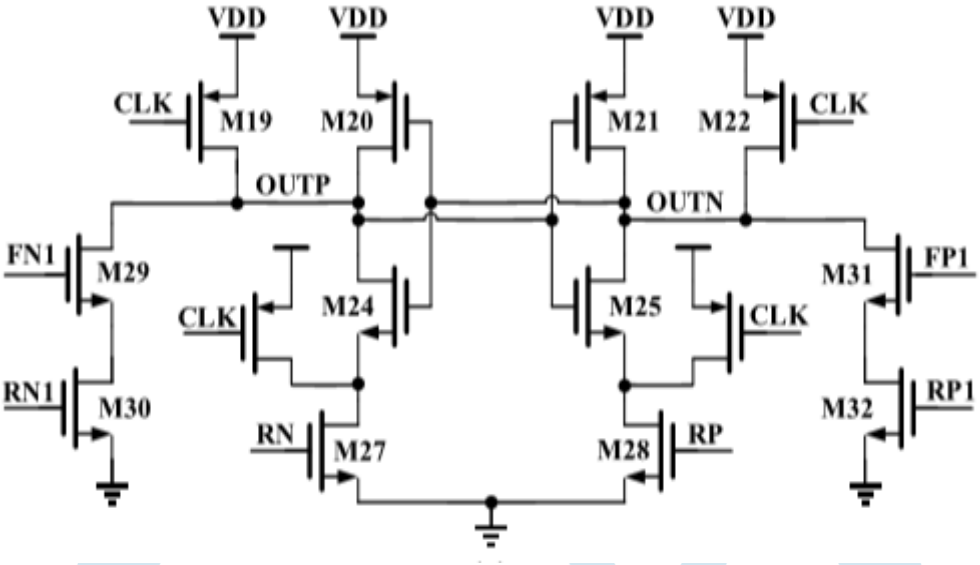


Fig: Proposed three-stage comparator. (a) Original 1st two stages with nMOS input (b) Extra 1st two stages with pMOS input (c) Third stage (latch stage).

ADVANTAGES:

The greater initial tiers of the proposed technique use pMOS enter pairs M11–12 to return out the nMOS enter M1–2 return noise. Furthermore, the greater routes M29–32 practice more signals to the latching OUTP and OUTN nodes , growing the regeneration pace even in addition.

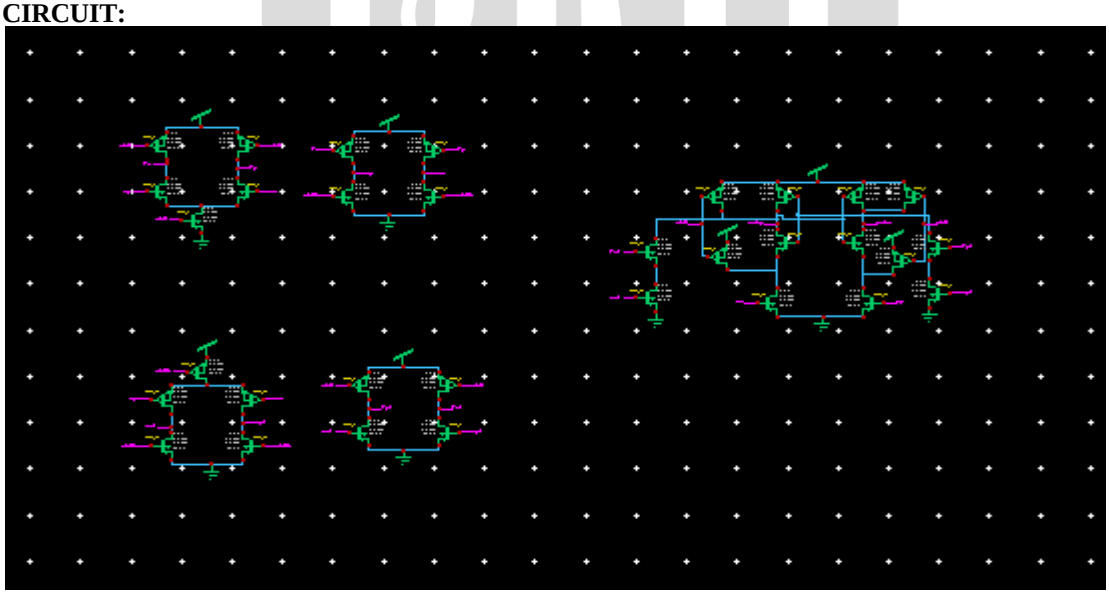
APPLICATIONS:

Comparator can be used in a variety of ways.

- They're found in audio and video equipment.
- They're found in mobile phones.
- They're commonly employed in mobile CMOS image sensors.
- They're employed in medical imaging and medical instrumentation.

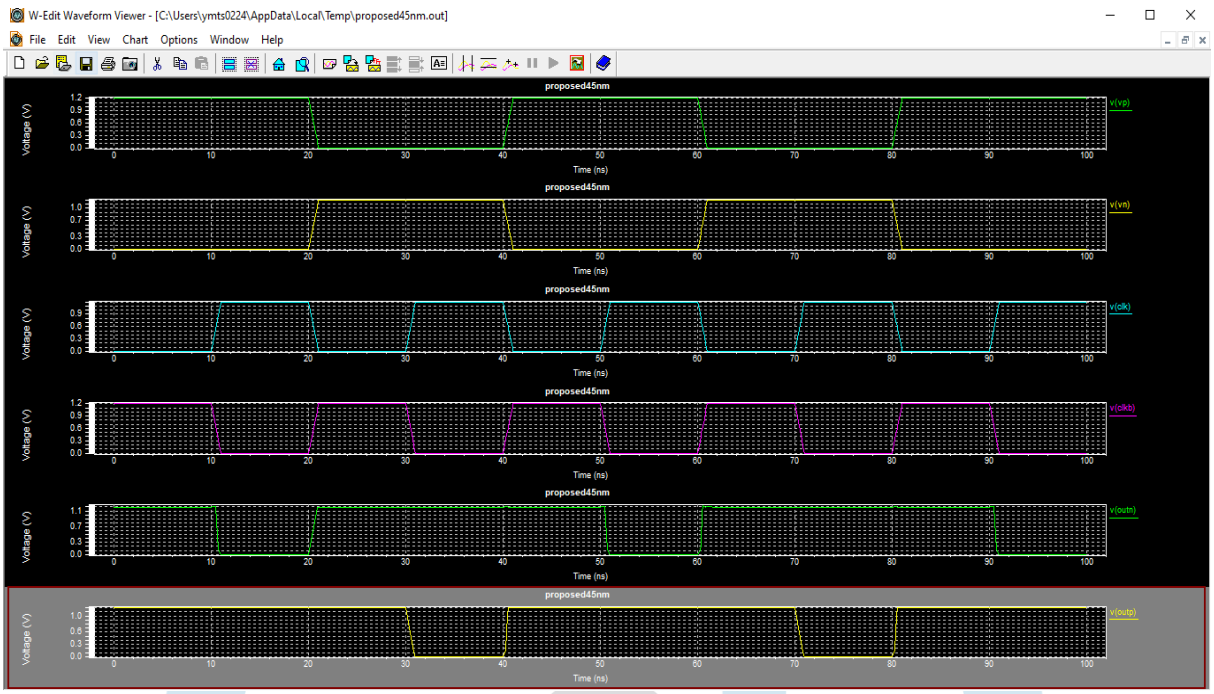
RESULTS

CIRCUIT:



Schematic diagram proposed modified comparator

OUTPUT WAVEFORMS :



Waveform of proposed comparator

Table: Evaluation of power, delay, area parameters

	AREA	**DELAY**	**POWER**
EXISTING	19	0.6	3.1
PROPOSED	32	0.4	5.4

CONCLUSION:

This article describes a three-stage comparator and a modified version of it, both of which having the advantages of high speed and low kickback noise. These comparators are ideal for SAR ADCs with high speed and high resolution. Finally, measured results back up the comparators 'effectiveness. Tanner EDA was used to implement all of the designs on 45 nm technology.

FUTURE PLANS:

The static power consumption, which is a major concern, can be further decreased by using low-power techniques for the suggested comparator design.