# Implementation of NAND Flash Memory Using Adiabatic Logic Circuit

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***Abstract*—To evaluate the NAND flash memory model I proposed the switching-voltage detector circuit and compensation circuits for low-voltage CMOS inverter. The switching voltage of inverter is an vital parameters in a digital circuit, and it is decided by way of the threshold voltages distinction between MOSFETs.The switching voltage is varying in a fabrication manner . To discover this problem, I developed a threshold voltage detector circuit. Here I additionally carried out the adiabatic logic circuits for decreasing energy dissipation in NAND flash memory .The adiabatic method reduces the energy dissipation during CMOS transistor switching events.I generally targeted to decrease the whole power consumption in NAND flash memory model.**

**Index Terms— NAND Flash,Adiabatic,CMOS,power dissipation, low power.**

## I. INTRODUCTION

NAND Flash memory is the kind of non-volatile technology.NAND is particularly used in USB drives and memory cards. NAND Flash memory generally used in our mobile telephones , smart televisions ,Laptops and tablets. It also observed in all traffic lights display system and digital advertising and marketing panels.NAND Flash technology offers the cost-effective solutions for high density storage. The switching voltage of the inverters decided by the voltage difference between the MOS transistors. The switching voltage is varying throughout the fabrication .To address that problem I implemented the voltage detector circuit. That circuit detects the voltage difference of the MOSFET in this circuit. Threshold voltage detector circuit was once monitor the threshold voltage distinction between nMOSFET and pMOSFET, and then switching voltage is decreased fifty percentage in inverter. Today another one primary problem in that NAND Flash memory circuit is energy consumption. Here I implemented the adiabatic logic approach to minimize the total energy consumption in this design. Adiabatic circuit is connected to the MOSFET transistors. During transistor switching some energy dissipation happened. To keep away from that problem I used adiabatic circuit to minimize that energy dissipation. So I achieved less energy consumption compare to previous NAND flash memory design .

CMOS transistors are dissipating the power when it switched. Adiabatic logic circuit provides a way to reuse the energy stored in the capacitor, rather than discharging the capacitor to the ground . Operations of adiabatic logic circuits are primarily based on some rules such as never turn on a transistor when there is a voltage between the source ,drain terminals, and it never changes the voltage across any of the CMOS transistors.

## II. WORKING:

Circuit diagram of NAND flash memory model shown in the fig 1.This circuit consists of three-stage CMOS inverters. The output reference voltage VREF of the detector circuit is applied to the supply voltage of the first inverter. However, because compensation is performed by voltage scaling based on the on-chip detector's signal, the "high" level of the first inverter varies according to the supply voltage. To solve this problem, a fixed digital supply voltage VDD, is used for the other inverters. The second and third inverters are normal CMOS inverters. However, because the logic function of the first inverter is already performed and the output voltage V1 is evaluated as "high" or "low", the effect of threshold voltage variations in the second and third inverters on the switching voltage is minimal.Here all the CMOS inverters dissipate power .To avoid that I implemented the adiabatic logic circuit in the CMOS inverter circuit.The capacitor added to the both the CMOS inverters .It reduces the power dissipation and total power consumption of the design also reduced.

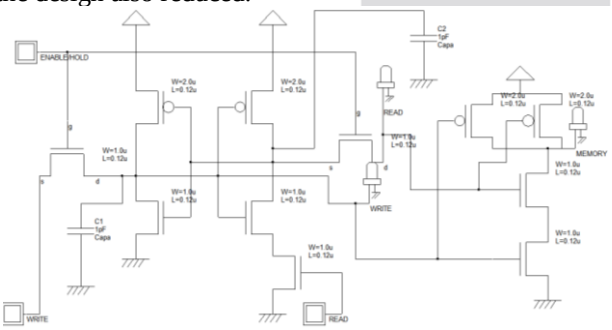


Fig.1.NAND flash memory circuit diagram

## III. RESULTS AND DISCUSSION:

The simulation diagram for write operation shown in Fig.2 and the simulation diagram for Read operation shown in Fig.3.Here we provides the LED for indicating the Write and Read operation.whenever the write operation is performed in then it writes data in NAND flash memory and for Read operation it read the data from NAND flash memory.

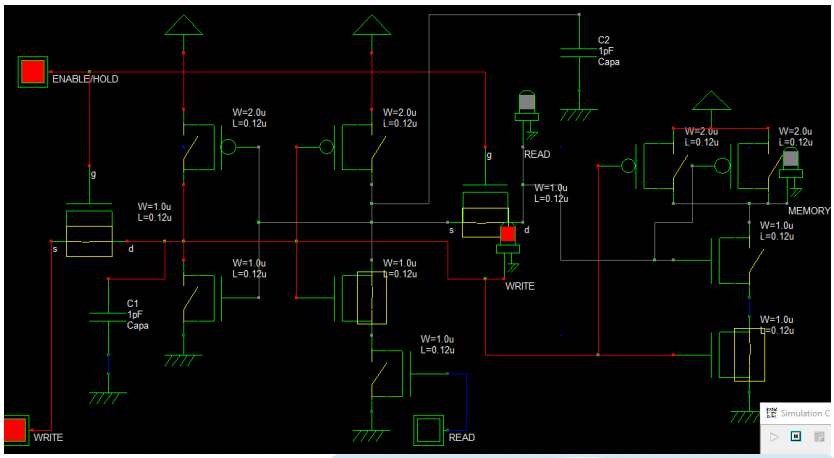


Fig.2.Write operation simulation diagram.

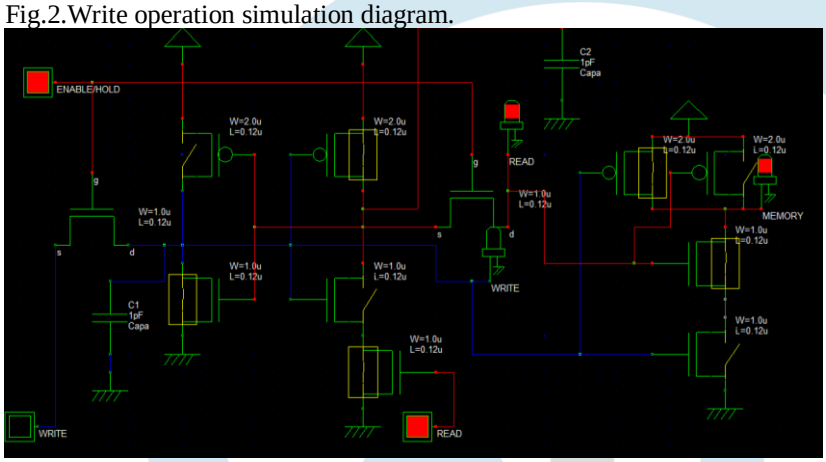


Fig.3.Read operation simulation diagram.

The simulation result waveform shown in Fig.4.For both Read and Write operation result is displayed here. Voltage vs current simulation waveform shown in Fig.5.The layout diagram of NAND flash shown in Fig.6.

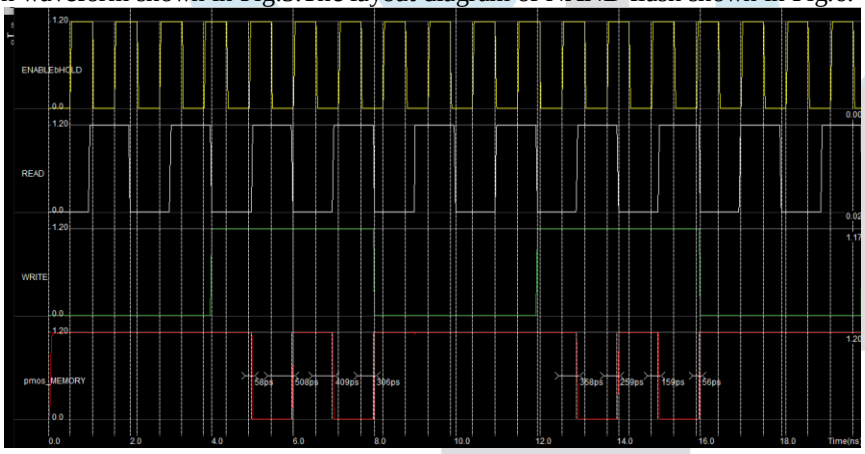


Fig.4. simulation waveform for both read and writes.

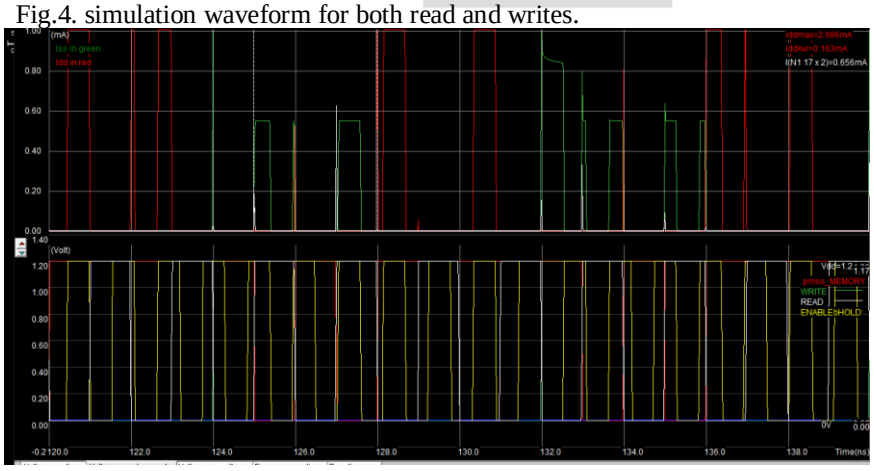


Fig.5. Voltage vs Current waveform.

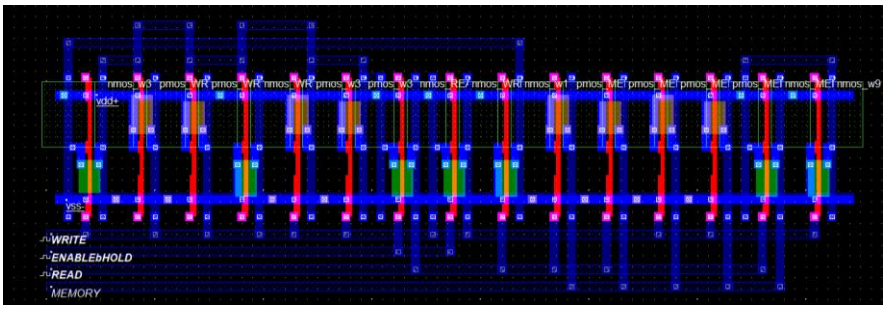

Fig.6. Layout Diagram for NAND flashes memory.

**CONCLUSION:**

The study says that the adiabatic logic circuits can considers as a main task in designing applications for which power consumption is the significant role like performance in any digital portable systems that running with batteries examples tablets, laptops, computers, mobile phones . Here I reduced the total power consumption of NAND flash memory. With an adiabatic logic circuit method, a pull-down circuit can consume more energy rather than the dissipated through as a heat. In future depending upon the requirements and its applications a suitable adiabatic logic circuit will be selected then designed to reduce the total power dissipation of such kind of systems.

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