High-Speed and Low Power 8T Full Adder Using 3T Ex-OR and 2T Multiplexer

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***Abstract*: Full adder circuit is one of the most important digital functional blocks used in Arithmetic and Logical Unit. Adders are the core element of arithmetic operations like addition, multiplication, division, exponentiation etc. In most of the systems adder lies in the critical path that affects the overall speed of the system. This paper presents a novel design of 8T full adder, which is designed on the logic of two 3T XOR and one 2T MUX, so in total of 8 transistors. Compared to other existing 14T, 10T, 9T Full adders the proposed design has significant improvement in power consumption, delay and power delay product. The proposed 8T full adder is implemented using the 90nm technology library and is simulated & verified using the DSCH simulation tool and 3D layout of 8T full adder is designed using Microwind tool. And it observed from the simulation results that the proposed 8T full adder has better performance than the other existing full adders in terms of power consumption, delay PDP (power delay product) and transistor count.**

Index Terms: 8T Full Adder, high speed, low power.

I. INTRODUCTION

In this modern world each and everything is getting upgrade to digital form which means portable electronic gadgets usage is getting increased day by day, such as cellular phones, personal digital assistants (PDAs), and notebook. For designing best out of these electronic systems, designers strive for small size, high speed, and low operating power circuits. VLSI designer need to consider area, performance, cost and reliability of the device. Power consumption had the secondary importance. But nowadays, the demand for the low power designs has been increasing tremendously. This kind of increasing demand has been due to the fast growing of portable electronic devices such as smart phones, smart watches, notebooks and laptops. These portable communication devices which require high speed and complex functionality with lower power consumption. Excessive power dissipation in integrated circuits reduce their use in these portable device applications. These electronic applications mostly comprise arithmetic circuits.

An adder is a fundamental component of most of the arithmetic circuits such as multipliers, program counters etc... These arithmetic circuits are extensively used in the data paths consuming almost one-third of power in the high-performance microprocessors. Therefore, by improving the overall performance of the adders, which improves the overall performance of the complete system. To understand a full adder (FA) circuit, various static CMOS logic styles have been presented. These logic styles can be broadly classified into two categories: classical design style and hybrid design style.

High power systems usually run hot, and this increase in temperature leads to failure in several silicon components. To control the temperature levels, the chip need specialized and costly packaging and cooling arrangements, which results in further increase in cost of the system. These impacts of high-power force the VLSI designers towards low power consumption in chips. While reducing the power consumption also we need to reduce delay of the circuit.

The total power dissipation in a circuit is consists of two components,
they are static and dynamic power dissipation. Dynamic power plays the major role in the power dissipation of complementary metal oxide semiconductor (CMOS) VLSI circuits.

Power(average) = Power(dynamic) + Power(static).

The Power can be reduced in different levels, either in system level or architecture level or algorithm level or micro architecture level or gate level or circuit level. Here the circuit level power reduction is proposed. In digital adders, the speed of addition of the binary numbers are limited by time required to propagate a carry through the adder. sum of each bit in a basic adder is generated sequentially (starting at the lowest order bit position) only after the previous bit has been summed and a carry (if generated) is propagated into next bit position. There are several types of adders available, we need to select which one is suitable of our device. In order to design the adders, single bit full adder is basic element. So, the selection of 1-bit full adder based on power, delay and area is necessary to build other type of adder circuits.

II. WORKING:

In the proposed 8T full adder sum is generated using two 3T XOR module, and carry is generated using NMOS and PMOS pass transistor logic devices. The equations are modified so as to visualize the 8T full adder design. The equations for 8T full adder design are:

SUM= A xor B xor C = (A xor B) xor C
CARRY=AB+BC+CA = AB+BC (A+A`) + AC (B+B`)
=AB+ (A xor B) C = (A`B) B`+ (A xor B) C

Instead of using two NMOS pass transistor devices we have used one NMOS and one PMOS pass transistor device, because of ease of the design and as according to the equation as shown above

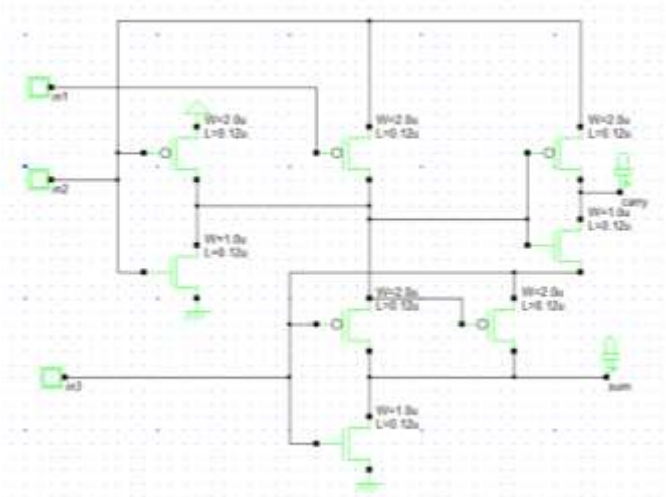

Fig.1 8T Full Adder circuit diagram

It must be noted that PMOS transistor passes ' l' clearly, but cannot pass '0' completely thus, the carry output has weak '0'. NMOS transistor passes '0' very precisely, but cannot pass '1' completely therefore, the carry output has weak ' 1 ', Having weak '0' and '1' at carry outputs is one of the disadvantages of 8T full adder circuit and also the PMOS transistor count is high compared to NMOS transistor count. In practical situations, one solution for this problem is using an inverter at carry output, but this solution will increase the power and area of the circuit.

III. RESULTS AND DISCUSSION:

The simulation of the 8T Full Adder is shown in Fig.2. Here we have three inputs in1, in2 and in3 of the full adder and we provide the LEDs to indicate the sum and carry of the full adder. When we have only one input is high then the sum led will glow. whenever more than one input is high, then the carry led will glow. When three inputs are high both the sum led and carry led will glow. The simulation output waveform 8T Full Adder is shown in Fig.3 (voltage vs time) and Fig.4 (voltage vs current). The layout diagram of the 8T full adder is shown in Fig.5.

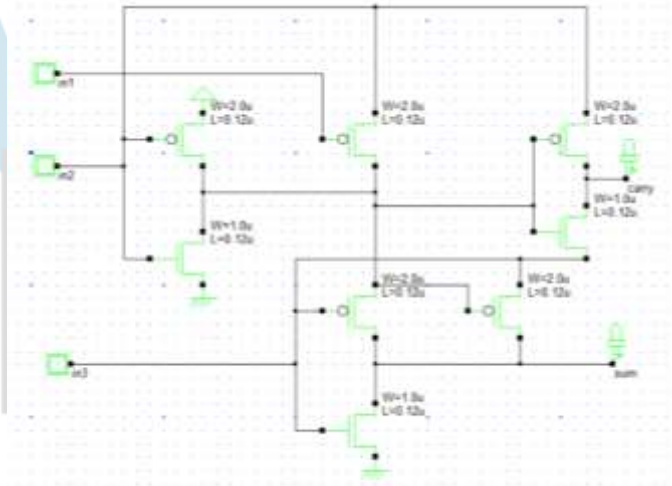

Fig.2 8T Full Adder simulation diagram

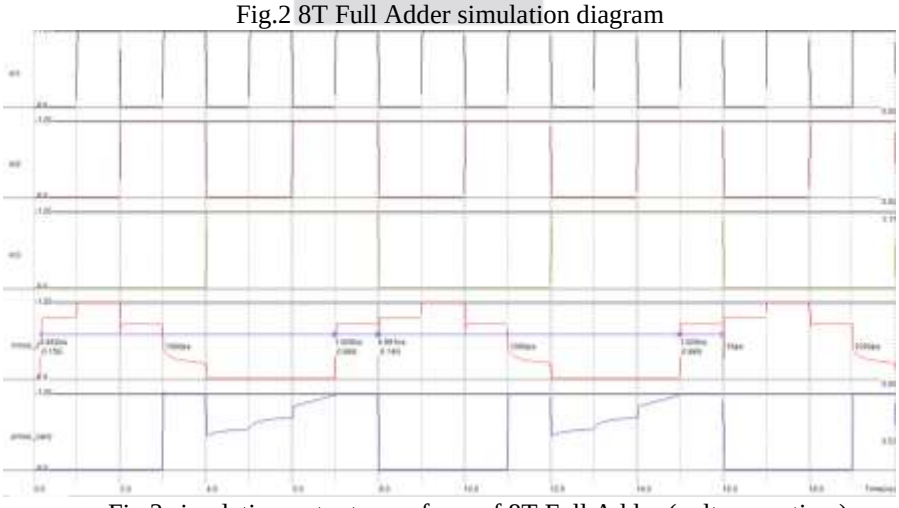

Fig.3 simulation output waveform of 8T Full Adder (voltage vs time)

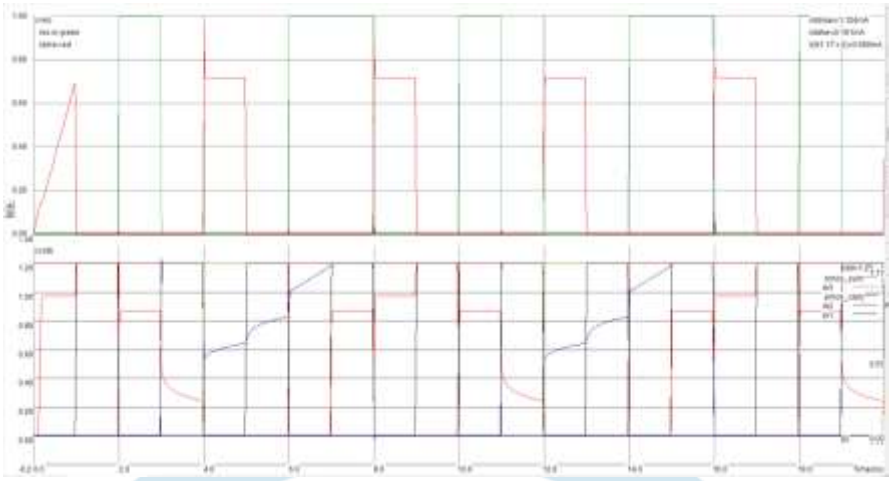

Fig 4. simulation output waveform of 8T Full Adder (voltage vs current)

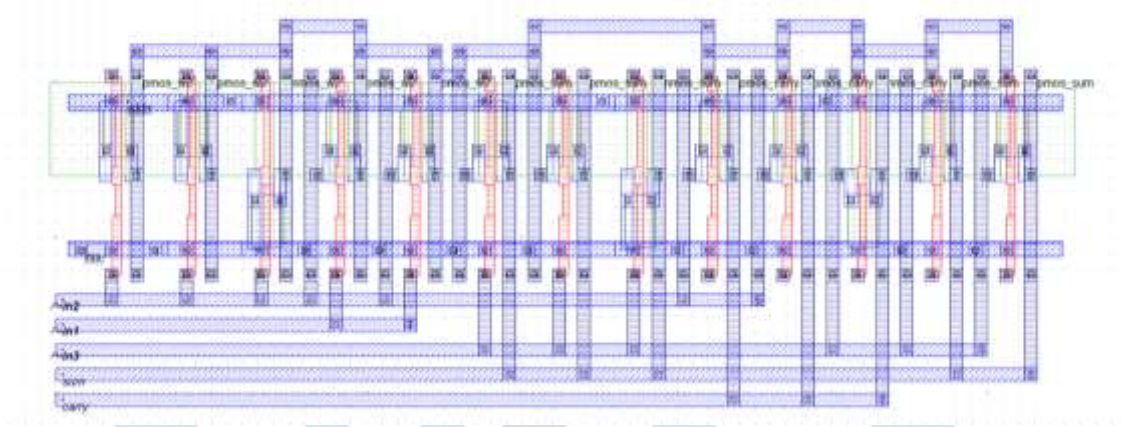

Fig.5 The layout diagram of the 8T full adder.

IV. CONCLUSION:

The proposed 8T Full Adder circuit is designed with 90nm technology and are simulated, analyzed and compared with other conventional 14T,10T and 9T Full Adders. The simulation result shows that the average power consumption is less than other conventional Full Adders. A smaller number of transistors used to design the proposed full adder circuit which reduced the power consumption and delay, when the delay is reduced the speed will increase automatically. The power consumption of the proposed full adder is 0.193uw lower than all other conventional full adder designs.

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