Design and Implementation of CMOS CS-Cascode Low Noise Amplifier

D.V.Prasad[1], RLBR Prasad Reddy[2*], Dr. Mahesh Mudavath[3]

[1]M.Tech Scholar, VLSI System Design
Dept. of ECE, Srinivasa Institute of Technology, Kadapa (A.P), India-516002
[2]Assistant Professor, Srinivasa Institute of Technology, Kadapa (A.P), India-516002.
[3]Professor, Jayamukhi Institute of Technological Sciences, Warangal

***Abstract*: This paper outlines the design process for a cascode Common Source stage with Inductive Degeneration (CS-ID) LNA that runs at 2.4GHz in 65nm CMOS technology. At a supply voltage of 1V, this chosen architecture offers a high power gain of 25dB and noise figure < 2.6dB. The cascode CS-ID gives perfectly matched with input/output impedance of 50Ω and it is verified with input & output reflection coefficients S_{11} = -15.1 dBm & S_{22} =-16.2 dBm. The low noise amplifier is intended for use as the cascode stage of a wireless communication receiver. The simulations are done in cadence virtuoso SpectreRF. The IEEE 802.15.4 standard, also known as ZigBee, is a low-tier, ad hoc, terrestrial wireless protocol that is somewhat comparable to Bluetooth. It can be utilised with the cascode stage because of its high gain and low noise figure.**

Index Terms: Low Noise Amplifier, Radio Frequency, cascode CS-ID, power gain, noise figure, CMOS scaling, 2.4GHz Frequency, ZigBee, Bluetooth, IEEE 802.15.4 standards.

1. INTRODUCTION

The wireless communications sector is now expanding incredibly quickly. Numerous thorough studies on CMOS radio-frequency (RF) front-end circuits have been conducted in response to the desire for a low-cost but high performance wireless front-end. The ultimate objective is to reduce the trade-off between high performance and inexpensive, low-power architecture [3].

The initial stage of a receiver is often a low noise amplifier (LNA). Its performance has a significant impact on the receiver's overall performance [1]. This study proposes an inductive degeneration LNA topology with a cascode Common Source stage. It is made to work with the IEEE 802.15.4 standard, which uses the 868 MHz, 915 MHz, and 2.4 GHz bands. Because it is an unlicensed band and is widely used, the well-liked 2.4 GHz industrial, scientific, and medical (ISM) spectrum was selected for this project. ZigBee, also known as the IEEE 802.15.4 standard [7], is a low-tier, ad hoc, terrestrial wireless protocol somewhat akin to Bluetooth [2].

One use for this kind of LNA is as the amplification stage in the receiver chain before the active mixer. A small amount of dc power is used by active mixer while it offers active gain. The gain criteria for the LNA can be loosened as a result. However, it must have a low power consumption to make up for the active mixer's high power consumption. To prevent lowering the total receiver NF, the LNA should have good NF with a relaxed gain. The gain of the cascode CS LNA has been maximized [9]. The receiver system, which uses a passive mixer for frequency conversion, can benefit from this enhancement. A passive mixer has some conversion loss but doesn't use any dc power. Therefore, in this kind of system, a high LNA gain is necessary. To validate the design process, the circuit's input matching, NF, and gain have been calculated.

This work uses 65nm technology in cadence to construct a low noise amplifier for RF front end with high gain, low noise figure, and excellent input and output impedance matching. LNA's main challenge is to deliver greater performance. This essay is below. The Low Noise Amplifier Concept is presented in Section II. LNA design considerations are included in section III. Results of the LNA design and simulation are presented in section IV. The job is finally concluded in section V.

2. CONCEPT OF LOW NOISE AMPLIFIER

Modern wireless systems may deliver signals in the sub-microvolt range, which emphasises the urgent requirement for low noise amplification. In the RF front-end module depicted in Figure 1, the low noise amplifier is the element that is most crucial for compensating for noise figure. Excellent gain, low noise figure, and high linearity are the main LNA design criteria [2,4,6]. Modern digital wireless systems use complicated digital modulations with high peak-to-average ratios for RF signals, making linearity increasingly crucial. As a result, a wireless receiver must have a very linear LNA to minimise inter-modulation distortion [11]. The 3rd order intercept point of the LNA's input refers to the linearity of the LNA. LNA should therefore increase the target signal's power while introducing the least amount of noise and distortion possible to enable the system's later stages to retrieve the signal [8, 10].

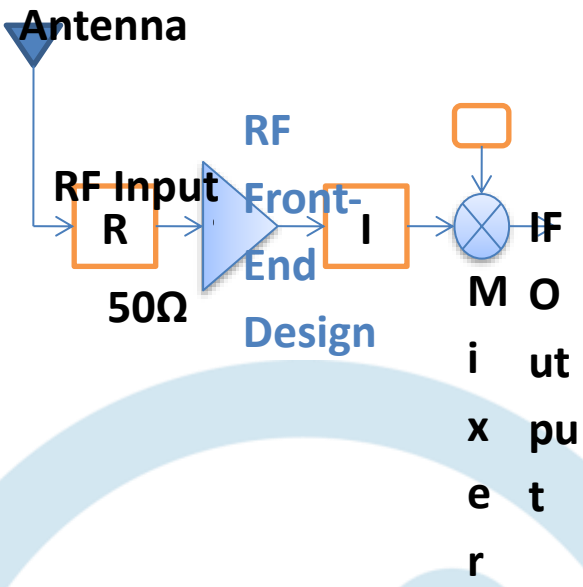

Fig. 1: Radio Frequency front-end receiver block diagram.

Because of its high gain and low noise, the CS LNA is frequently utilised for narrow-band applications. The value of the inductor connecting the source terminal to ground, however, is typically fairly modest and sensitive to process fluctuation due to the input matching condition. Additionally, because not all inductor values are included in the Process Design Kit, the requirement for a small inductor might occasionally present problems for the LNA design (PDK) [13].

2.1. DESIGN PARAMETERS OF LNA

The following design parameters are used to construct to the low noise amplifier.

- **Noise Figure**: This specifies the noise performance of a circuit or device. Noise Figure measures the SNR degradation as a signal pass through a system. If a system has no noise the NF=1, F=0dB. The ratio of input SNR to the output SNR it can be expressed as

$$\text{NF} = \frac{\text{SNR in}}{\text{SNR out}}$$

Where SNR denotes the signal-to-noise ratio at a particular node, as the LNA is the first block of the receiver, its NF decides the NF of the entire receiver chain. Noise figure of an LNA is considered to be less than 3dB.

- **Gain:** Gain of LNA should be large enough to minimize the noise contributions of subsequent stages. However, the choice of gain leads to a compromise between noise figure and linearity, as high gain may saturate subsequent devices.
- **Input Return Loss (input matching):** For maximum power transfer from the antenna and the LNA, the input return loss (S_{11}) of the LNA should be low; else the antenna will reradiate part of the input signal [14, 15, 16].
- **Stability:** The LNA should be stable of all source impedances at all frequencies. If the LNA begins to oscillate at any frequency, it becomes heavily non-linear and its gain becomes highly compressed. A measure of stability is Stern stability factor and defined as [17,18,19],

$$k = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12} * S_{21}|)$$

Where
$\Delta = (S_{11} * S_{22} - S_{12} * S_{21})$. If K > 1 and $\Delta < 1$, the circuit is unconditionally stable.

- **Linearity:** Linearity of the LNA is defined by its IP_3 and P_{1dB} points. The LNA does not limit the linearity of the receiver. Owing to the cumulative gain through the RX chain, the overall IP_3 and P_{1dB} points are automatically limited. So in LNA design, its linearity is of least concern [20].
- **Sensitivity:** It can be define as minimum signal level that a system can detect with acceptable signal-to-noise ratio at the output. It can be expressed as [21,22,23].

$$P_{in\ min} = \left[-\frac{174\ dBm}{Hz} + NF + 10logB\right] + SNR_{min}$$

- **Dynamic Range:** It can be defined as the ratio of maximum input level that the circuit can tolerate to the minimum input level at which circuit provides a reasonable signal quality [24].

$$DR = \frac{P_{in\ max}\ [dBm]}{P_{in\ min}[dBm]}$$

3. DESIGN CONSIDERATION OF LNA

This topology provides resistive input impedance at the resonant frequency without the thermal noise of an ordinary resistor and degrading the noise performance of the amplifier shown in Fig. 2.

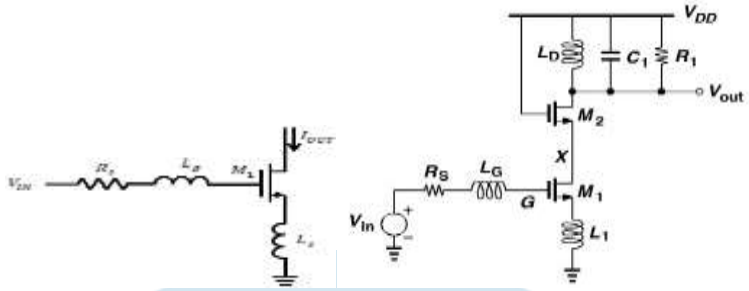

Fig. 2: Cascade CS stage with Inductive Degeneration

LNA (Low Noise Amplifier) of the RF Front-End is the main topic of this study. It must strike a compromise between noise figure and linearity in order to full-fill the design requirement. This proposed architecture includes source inductive degeneration LNA. And also it must meet the requirements of common design features for the receiver front-end like Noise Figure (NF), input-referred third-order intercept point (IIP_3) and input power 1-dB compression point (CP_{1dB}), and Conversion Gain. Low power consumption as well as good noise performance is a great challenge to design [1, 2].

Cascade CS stage with inductive degeneration of low noise amplifier design equations are [25][26],

- Input impedance $Z_{in} = R_g + R_{L1} + R_{Lg} + s(L_1 + L_g) + \frac{1}{sC_{gst}} + \frac{g_m}{C_{gst}} L_1$

$$Re(Z_{in}) = \frac{g_m}{C_{gst}} L_1 = \omega_T L_1 = Rs$$

$$Im(Z_{in}) = w(L_1 + L_g) - \frac{1}{wC_{gst}} = 0$$

The real part should be matched to 50 Ω and L_1 and C_{gs1} tuned to operating frequency. This constrains the values of g_m, L_1 and C_{gs1}.

A better solution is to add an inductor L_G. More freedom in choosing passives for input matching

- Gain $= \frac{\text{V out}}{\text{V in}} = \frac{\omega T\ R1}{2\omega o\ Rs} = \frac{R\ 1}{2L1\ \omega o}$

- $NF = 1 + g_m R_s \Upsilon \left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_1}\left(\frac{\omega_o}{\omega_T}\right)^2$

In this topology, isolation between the input and output resonant networks is better than other CS topologies where C_{GD} only presents the isolation.

- L_1 is generally realized through a bond wire between the source of M_1 and ground. Bond wire inductance varies between 1-2nH.
- $C_{GS}=\frac{g_m L_1}{R_S}$. For $g_m = 10mA/V$, L_1=2nH ; C_{GS} =400fF. For designs in lower technology nodes, external C_{GS} has to be used.

The common-source amplifier M1 and the common-gate device M2 make up the cascode common-source LNA, which is the topology just below. The device size is big for noise optimization, resulting in high input capacitance and low input impedance. Input signal will be attenuated because of low input impedance, hence input matching network comprising L_G and L_1 is constructed. L_D and C_1 is the output resonating network tuned to frequency of operation. R_1 is the parasitic resistance of the resonant network determining the gain of the LNA [27], [28].

A design strategy of a cascade CS LNA will be described in the following.

Design of the complete LNA with matching network is shown. The LNA is designed in 65nm CMOS technology and operates at 2.4 GHz with gain >20dB, S_{11} and S_{22}<-20dB and noise figure <3dB.

Some transistor parameters in 65nm technology are,

t_{ox}=2.6nm

μ_n=243 cm^2/V-s

V_{th}=0.36 V for L=250nm

The current consumption considering the power dissipated to be PD is,

$I_D=\frac{P_D}{V_{DD}} = \frac{2mW}{1V}$=2mA

Find out the oxide capacitance C_{ox},

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{sio2}}{t_{ox}} = \frac{\varepsilon_0 * 3.9}{2.6nm} = 13.275mF/m^2$$

For the LNA the power constrained noise optimized width of the transistors is given by,

$$W_{opt} = \frac{1}{3\omega_0 L C_{ox} R_s} = \frac{1}{3 * 2\,\pi * 2.4G * 250n * 13.275m * 50} = 133\mu m \approx 140\mu m$$

Find out the transconductance $g_m$of the transistors according to the formula,

$$g_m = \sqrt{2\mu_n \varepsilon_{ox} \frac{W_{opt}}{L} I_D} = 26.88 \text{ mA/V}$$

For input matching of the LNA, two conditions are to be satisfied,

$$R_S = \frac{g_m L_s}{C_{gs}}$$

$$(L_1 + L_g) = \frac{1}{wo^2 C_{gst}}$$

Thus C_{gst} can be found by,

$$C_{gst} = \frac{g_m L_s}{R_s} = \frac{26.88n * 2n}{50} = 1.0752pF$$

This C_{gst} represents the total capacitances across the gate-to-source of the input transistor [5]. However this transistor already has a junction overlap parasitic capacitances associated with it, which can be calculated as,

$$C_{gs\,mos} = \frac{2}{3} WLC_{ox} = 309.75fF$$

Thus to compensate for the extra C_{gs} , an external capacitance has to be connected.

$$C_{gs\,external} = C_{gst} - C_{gs\,mos} = 1.0752p - 309.75f = 765.45fF$$

L_g, the gate inductance, can be obtained from,

$$L_g = \frac{1}{w_0^2 * C_{gst}} - L_s = \frac{1}{(2\pi * 2.4G)^2 * 1.0752p} - 2n = 2.09\,nH$$

The gain of the LNA is 20dB. If R_P be the parallel parasitic resistance of an inductor operating at 2.4GHz, then the gain can be written as,

$$Gain = g_m R_P = 10$$

$$R_P = \frac{Gain}{g_m} = \frac{10}{26.88m} = 372\Omega$$

Q of an inductor model having a parallel resistance R_P is,

$$Q = \frac{R_P}{\omega_0 L_d}$$

Thus the load inductance and capacitance value can be calculated as,

$$L_d = \frac{R_P}{\omega_0 Q} = 3.9\,nH$$

$$C_d = \frac{1}{w_0^2 * L_d} = 1.127\,pF$$

A bias voltage has to be applied to the gate of the input transistor.

$$V_{GS} = V_{Th} + \sqrt{\frac{2I_D}{\mu_n \varepsilon_{ox} \frac{W_{opt}}{L}}} = 0.36 + 0.14 = 0.5\,V$$

The LNA is coupled to an output matching network for 50 Ω resistance matching. The parasitic parallel resistance of the LdCd network, R_P, serves as the LNA core's output resistance. R_P will be reduced to 50 Ω through the matching network..
The Q of the matching network is,

$$Q = \sqrt{\frac{R_p}{50} - 1}$$

The matching network inductance L_m is thus,

$$L_m = \frac{Q * 50}{w_0} = 10.4\,nH$$

The matching network capacitance C_m is thus,

$$C_m = \frac{1}{w_0^2 L_m} \frac{Q^2}{Q^2 + 1} = 383\,fF$$

4. LNA DESIGN AND SIMULATION RESULTS

This section displays the measured findings for the cascade common source CMOS LNA, which is using 65nm technology and operating at a 2.4 GHz frequency range. The measured Voltage Gain is 25dB, Noise Figure is 2.6dB, the input return loss (S_{11}) and output return loss (S_{22}) is -15 dB and -22.2 dB respectively shown in following Figures.

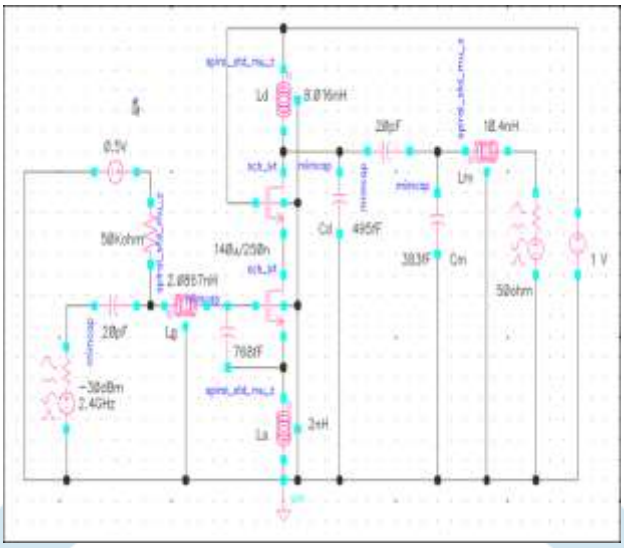

Fig. 3: Schematic of LNA Design

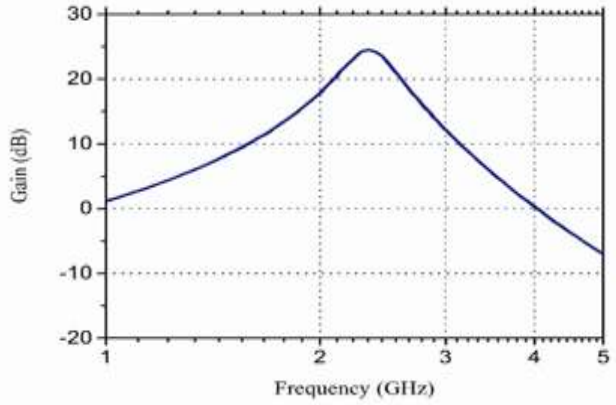

Fig. 4: Voltage Gain (dB)

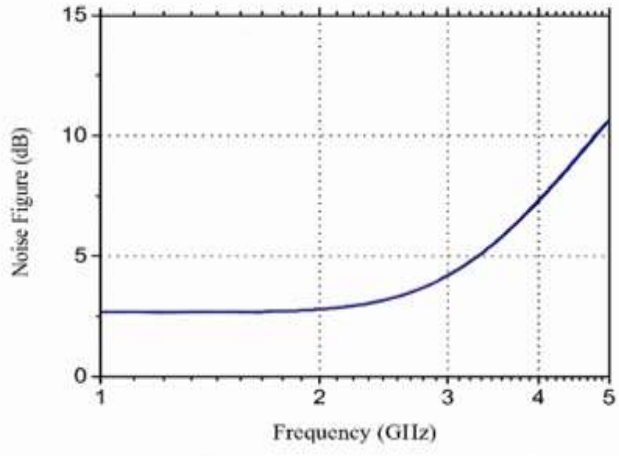

Fig. 5: Noise Figure (dB)

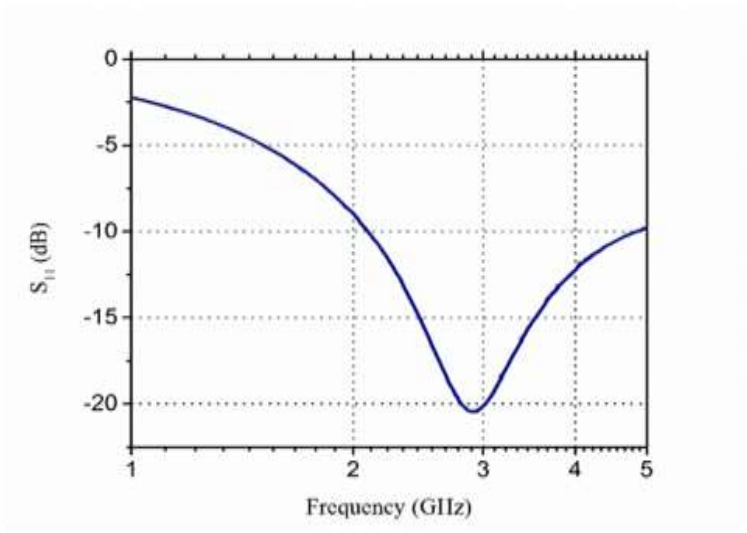

Fig. 6: S_{11} (dB) Parameter

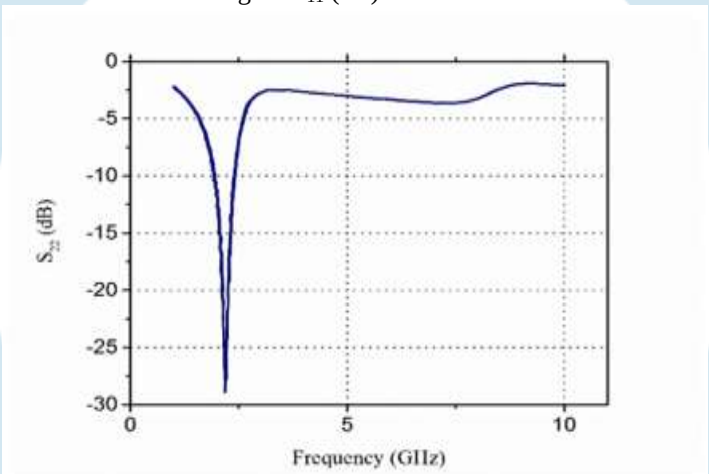

Fig. 7: S_{22} (dB) Parameter

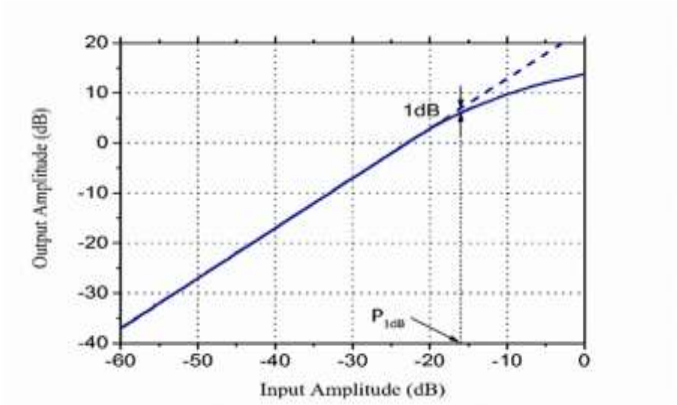

Fig.8: Fig. 8: P_{1dB} (dB) Point

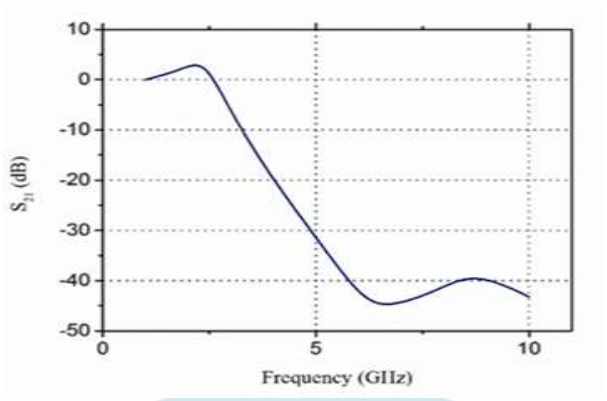

Fig. 9: S_{21} (dB) Parameter

5. CONCLUSION

In order to identify a method that can assist in achieving a low-power, compact, reliable, and fully-integrated LNA design, the design difficulties of cascade CS CMOS LNA, specifically for the IEEE 802.15.4 standard, are examined in great detail in this work.

Design challenges are described in detail, including performance trade-offs and input matching systems. Next, the IEEE 802.15.4 standard's LNA requirements are derived. This prompted us to suggest a number of design strategies that profit from the IEEE 802.15.4 standard's lenient performance criteria.

REFERENCES

1. S. Radha, Jisha Mathew, " Linearization of Low Noise Amplifier for Wireless Sensor Networks", IEEE International Conference on Inventive Systems and control, 2017 ISSN:978-1-5090-4715-4/17,pp.1-4,2017.
2. Vandana Kumari Chalka, Navaid Zafar Rizvi, "CMOS Low-Noise Amplifier for 2.4GHz wireless Receiver", IEEE international conference on Electrical, Electronics and Optimization Techniques, 2016, pp: 4235-4239.
3. M Mudavath, K. Hari Kishore, Azham Hussain and C.S. Boopathi "Design and analysis of CMOS RF receiver front-end of LNA for wireless applications", in "*Microprocessors and Microsystems*, Volume 75, 13th January. 2020, 102999 (SCI+ Scopus+ web of science)", doi: https://doi.org/10.1016/j.micpro.2020.102999.
4. Prameela B and Asha Elizabeth Daniel, "Design and Analysis of Different Low Noise Amplifiers in 2-3GHz" International Conference on VLSI Systems, Architectures, Technology and Applications, 2016.
5. Smrity Ratan, Debalina Mondal, Anima R, Chandan Kumar, Amit Kumar, and Rajib Kar, "Design of 2.4 GHz Differential Low Nosie Amplifier Using 0.18µm CMOS Technology" International Coference on Computing, Communication and Automation, pp:1435-1439, 2016.
6. Mingcan Cen and Shuxiang Song, "A low power 5.8GHz Fully Integrated CMOS LNA for Wireless Applications", SERSC International Journal of Hybrid Information Technology, Vol. No.1(2014), pp:157-166.
7. Mahesh Mudavath, K.HariKishore, "Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications" Asian Journal of Information Technology, Medwell Journal, Vol. No. 15, Issue No.20, pp:4040-4047, 2016.
8. Amra Fathima, Sushma P.S, Siddesh Gaonar, " Design of High Gain, Low Power CMOS Multi-Standard LNA" IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2016, India, pp:663-666.
9. Mahesh Mudavath, Sresta Valasa, Avunoori Saisrinithya and Amgothu Laxmi Divya "Design of Cryogenic CMOS LNAs for Space Communications", in Journal of Physics: Conference Series, Volume 1817, Issue 1, 2021, 012007, ISSN: 1742-6588, E-ISSN: 1742-6596, IOP Publishing, DOI: 10.1088/1742-6596/1817/1/012007.
10. Behzad Razavi, "CMOS RF Receiver Design for Wireless LAN Applications", Electrical Engineering Department, University of California, Los Angles. Page(s): 38-152.
11. Behzad Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's". IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 10, OCTOBER 1999.
12. John W.M. Rogers, Calvin plett. Radio Frequency Integrated Circuit Design, Artech House, London, ch.7, page.171.
13. M Mudvath, K.Hari Kishore "A Low NF, High Gain of 2.4GHz differential LNA design for wireless applications" in *International Journal of Scientific & Technology Research (IJSTR), VOL. 8, ISSUE 12*, pp: 109-116, December-2019, ISSN:2277-8616.
14. S.K Alam and Joanne DeGroat "A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications", 2006 IEEE, page(s):13-16.
15. Razavi. B, 1999. CMOS technology characterization for analog and RF design IEEE J. Solid State Circuits, 34: 268-276.
16. Razavi. B, 1998. RF Microelectronics Prentice Hall Publisher, New Jersey, USA, Pages.180.
17. Bosco Leung, 2011, "VLSI for Wireless Communications", second edition, Springer, Page(s):62-162.
18. T.Lee, The Design of CMOS Radio Frequency circuits, second edition ed. Prentice Hall, 2003.
19. B. L H. Rastegar and J.Y. Ryu, "A broadband Low Noise Amplifier with built-in linearizer in 0.13-µm CMOS process", Microelectronics Journal, Vol. 46, No. 8, pp. 698-705, August 2015.

20. M Mahesh and K. Hari Kishore "*RF Front-End Design of Inductorless CMOS LNA circuit with noise cancellation method for IoT Applications"* in *International Journal of Innovative Technology and Exploring Engineering (IJITEE)" Vol.8, Issue-6S, page: 176- 183, 2019,* ISSN2278-3075.
21. Wei, Y. J. Hossein Hadaian, Esmail Nagafi Aghdam and Javad Abbaszadeh, "A Dual Band Concurrent Low Noise Amplifier for Bluetooth and WLAN Applications", Journal of Engineering and Applied Sciences, pp172-175. 2016
22. Dai, X. X. Zhang, and Y. J. Lu, " A 2.4 GHz low-IF front-end receiver in 0.18-µm CMOS for IEEE 802.15.4 WPAN applications", *IEEE 8th International Conference on ASIC*, Changsha, Hunan, p. 1137 - 1140, Oct. 2009.
23. Jan Magne Tjensvold, "Comparison of the IEEE 802.11, 802.15.1, 802.15.4 and 802.15.6 wireless standards."
24. Mudavath M and K. Hari Kishore "*Design and Analysis of Receiver Front-End of CMOS cascode common source stage with inductive degeneration low noise amplifier on 65nm technology process" Journal of computational and theoretical nanoscience (JCTN)" Vol.16, No.5-6, page: 2628-2634, May-2019,* ISSN 1546-1955 (Print); ISSN 1546- 1963(Online).
25. Amgothu Laxmi Divya, Mahesh Mudavath, Ch S Ranadheer, Mohamed Afzal and R.Venkateswarlu "Low Noise Amplifier Design and Performance Analysis of RF Front-End for Narrow Band Receivers", in Journal of Physics: Conference Series, Volume 1817, Issue 1, 2021, 012005, ISSN: 1742-6588, E-ISSN: 1742-6596, IOP Publishing DOI:10.1088/1742-6596/1817/1/012005.
26. Thurpati,S., Mahesh M, Muthuchidambaranathan, P. "Performance analysis of linear precoding in downlink based on polynomial expansion on massive MIMO systems" in Journal of Physics: Conference Series, Volume 2062, Issue 1, 2021, 012006, ISSN: 1742-6588, E-ISSN: 1742-6596, IOP Publishing, DOI: doi:10.1088/1742-6596/2062/1/012006.
27. Sresta Valasa, D.R.Ramji, Jitesh Shinde and Mahesh Mudavath, "An improved impulse noise removal VLSI architecture using DTBDM method", in Springer Lecture Notes on Data Engineering and Communication Technologies, Vol. 63, pp: 325-335, Series Ed.:Xhafa, Fatos, ISSN: 2367-4512, 2021, DOI: 10.1007/978-981-16-0081-4_32
28. MM and K. Hari Kishore "Low Noise Amplifier Design of CMOS Inductorless with Noise Cancellation Technique" in *International Journal of Engineering and Advanced Technology (IJEAT),* ISSN: 2249–8958, Volume-9, Issue-1, October 2019, pages1537-1542.