Design and Analysis of SRAM cell with PMOS Access Transistor

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***Abstract*: Devices with low power consumption are essential in the present electronic era of circuit shrinking. Power consumption is one of the difficult variables that has an impact on the design of small devices and high-performance ICs. The typical SRAM cell designs are power-hungry and unimpressive in this new era of quick mobile computing. The power consumption of low power SRAM cell designs has been examined in this study. Conventional 6T SRAM cell, Gated VDD and Stacking based SRAM cell is designed using PMOS access transistors. The design is implemented and analyzed for static power consumption at 45nm technology in Cadence Virtuoso. Gated VDD using PMOS access transistors shows reduced static power when compared to above SRAM cells.**

***Index Terms*: Cadence, Gated VDD SRAM Cell, low power, PMOS access transistor**

I. INTRODUCTION

As a result of increased demand for portable devices, scaling down of CMOS technology has rapidly increased in recent years. Sub-threshold leakage is caused by CMOS scaling technology. Short channel effects, gate dielectric leakage, and device to device variances also contribute to leakage. Additionally, the SRAM unit houses the most of the transistors on a device. As cache memory employs an array architecture, a single SRAM cell's reduced power consumption can result in significant power savings for the entire system. Reverse-biased junction leakage current, sub-threshold leakage current, and random leakage current are the main sources of static power dissipation in CMOS transistors. Sub-threshold leakage and are two of these. The predominant currents in an SRAM cell are gate leakage currents.

Conventional 6T SRAM cell is the most used SRAM cell because of simplicity in its design. However, this type of architecture of SRAM cell results in large power dissipation in the cell. Hence different techniques are proposed to reduce the leakage power of the SRAM cell thereby reducing the overall power consumed by the cell.

In paper [1], different architectures of SRAM cell such as MTCMOS and Gated VDD is implemented. All the architectures are then analysed to obtain the power dissipated by the SRAM cell. The results show that MTCMOS consumes lesser power as compared to Gated VDD SRAM cell.

SRAM cell is implemented in which Leakage noise and improves power consumption in SRAM cell[2].

In paper [3], A low power 7T SRAM cell is implemented by using I-SVL circuits. The results show that large amount of leakage power is reduced by this technique when compared with USVL and LSVL techniques.

two TCAM cells are implemented one using 6T SRAM cell and another using 8T SRAM cell in order to minimize the power consumed by the TCAM cell. This was simulated at 90nm CMOS technology using Cadence Virtuoso[4].

In paper [5] and [8], different techniques to implement SRAM cell is used such as MTCMOS in [5] and VTCMOS in [8]. In [8], VTCMOS technique is applied to conventional 6T SRAM cell and it was observed that VTCMOS shows 34.59% of static power reduction in comparison to conventional SRAM cell.

II. CONVENTIONAL 6T SRAM

In fig 1, a typical 6T SRAM cell is displayed. Two cross-coupled inverters make form a 6T SRAM cell, and NMOS pass transistors are employed as access transistors. The inverters act as a storage component by holding the data bit in the SRAM cell as long as there is power.

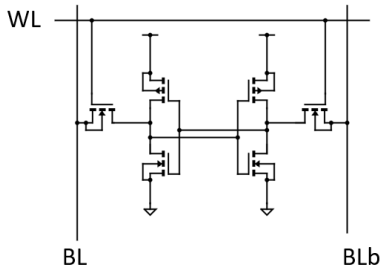

Fig 1 : Conventional 6T SRAM cell

A. HOLD mode:

As long as there is power supply, the data will be retained in the cell. Both of the NMOS access transistors are OFF when the word line, WL=0. As a result, the data will be kept in the cell. Standby current is the name of the current used in this mode.

B. WRITE mode:

During this mode, the data will be written onto the SRAM cell when word line WL=1. Bit lines BL and BLb are complementary bits used on either side of the NMOS access transistor cells. The bits are complementary to each other and this is done to ensure that the load to charge is minimised for each access transistor. Once the data is written onto the cell, the word l ine WL is made to be equal to 0 so that the access transistors are OFF.

C. READ mode:

When word line WL=1 in this mode, the data will be read from the SRAM cell. Pre-charges to VDD will be applied to bit lines BL and BLb. The amount of data stored in the SRAM cell will determine how slowly the bit lines are discharged.

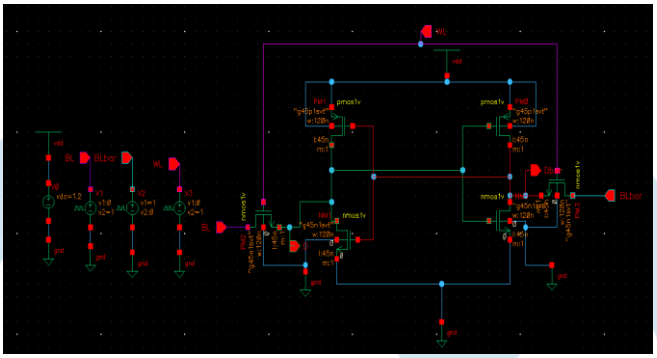

Fig 2: 6T SRAM cell

Fig 2 shows the implementation of 6T SRAM cell in Cadence Virtuoso using 45nm technology with a power supply of 1.2V.

Fig 3: Simulation waveform of 6T SRAM cell

During switching activity, the power consumed is given by equation (1)

$$P_{SWITCHING} = \alpha * f * C * V_{DD}^2 \quad (1)$$

Where α is the activity factor, f is the frequency of operation, C is the load capacitance and V_{DD} is the supply voltage.

Second is the SC power dissipated from V_{DD} to ground when both NMOS and PMOS transistor operate simultaneously and is given by equation (2)

$$P_{SHORT} = V_{DD} * I * t_{SC} \quad (2)$$

Third power dissipating source is the static power consumed when both NMOS and PMOS transistors are in OFF state and is given by equation (3)

$$P_{STATIC} = V_{DD} * I_{LEAK} \quad (3)$$

III. POWER REDUCTION TECHNIQUES FOR SRAM CELL

A Conventional 6T SRAM cell uses two NMOS access transistors. The static power consumed by NMOS transistor is higher than that of PMOS transistors. Therefore, this paper uses PMOS as access transistors in order to analyse the static power consumed by the different architectures of SRAM cell such as Gated VDD and transistor Stacking based. The simulation is carried at 45nm CMOS technology using Cadence Virtuoso.

A. Gated VDD

When the SRAM cell is not in use, the supply voltage is turned off in Gated VDD, preventing any leakage current in the OFF state. This reduces the SRAM cell's power dissipation. PMOS access transistors can be used to implement and analyse the Gated VDD mechanism of SRAM cells.

When word line WL=1, the PMOS access transistors are OFF as a result the cell remains in hold state.
When word line WL=0, the PMOS access transistors are ON as a result the data in Bit line is written in the cell.

There is a use of an additional NMOS transistor at the ground which acts as a control mechanism to block the supply voltage when the SRAM cell is OFF. Static power dissipated by the cell is calculated keeping the access transistors in OFF state i.e when there is no switching activity in the cell and the bit lines are kept complementary to each other. Fig 4 shows the implementation of Gated VDD SRAM cell using PMOS access transistors. Fig 5 shows the simulation of the same.

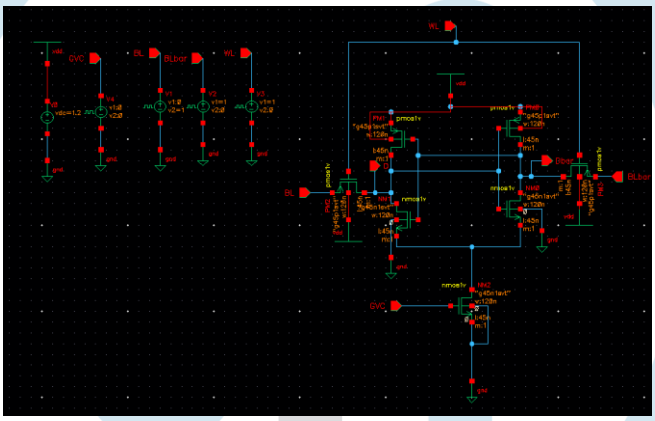

Fig 4: Gated VDD based SRAM cell

Fig 5: Simulation waveform of Gated VDD based SRAM cell

B. Transistor Stacking

In transistor stacking based SRAM cell, the transistors are stacked one on top of the other by reducing the width of each other by half.

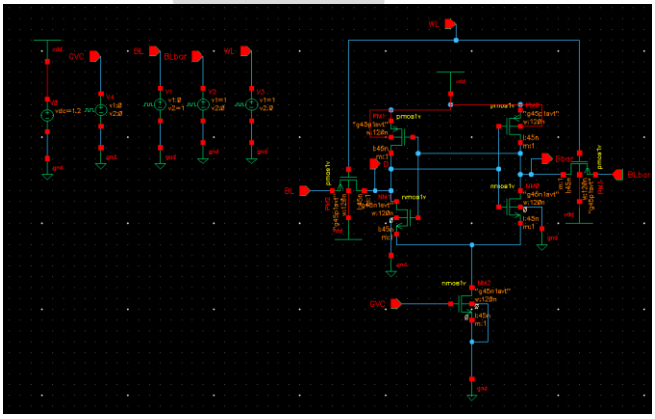

Fig 6: Transistor stacking based SRAM cell

This technique lowers the sub-threshold outflow current by maximizing the source voltage of the top most transistor in the stack and reducing the gate to source voltage of the lower transistor in the stack as shown in figure 6. The access transistors used here are PMOS transistors in order to analyse the power consumed by the cell.
Fig 7 shows the simulation results of the transistor stacking based SRAM cell. The supply voltage used is 1.2V.

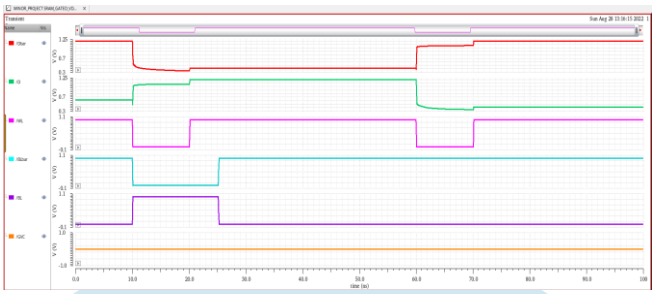

Figure 7: Simulation waveform of Transistor stacking based SRAM cell

Fig 7 shows the simulation results of the transistor stacking based SRAM cell. The supply voltage used is 1.2V.

IV. RESULTS AND CONCLUSION

Table 1 : Static Power Analysis and Delay

SRAM CELL TYPE	STATIC POWER DISSIPATED (PW)	DELAY (PS)
6T SRAM CELL	105.6336	358.5
GATED VDD	97.791	335.8
TRANSISTOR STACKING	99.277	146.7

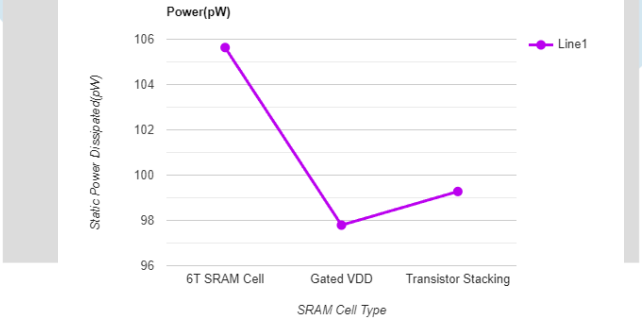

Fig 8: Graph between Static Power vs SRAM cell type

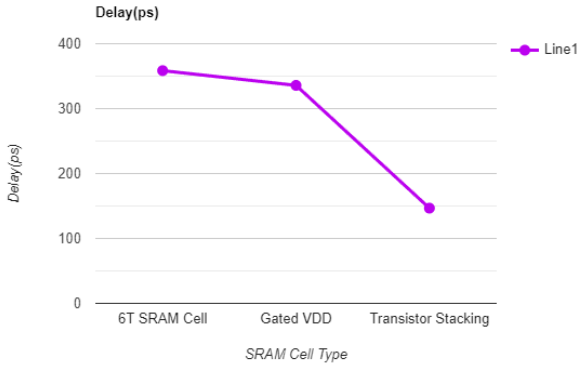

Fig 9: Graph between Delay (ps) vs SRAM Cell Type

Table 1 shows the static power dissipated by the PMOS based SRAM cells. The SRAM cells were implemented using Cadence Virtuoso at 45nm CMOS technology. The power supply provided is 1.2V. Width and lengths of the transistors are kept at default for the Gated VDD technique. The width in Transistor stacking is made half the default value. From the on top of table it's determined that Gated VDD dissipates to 6T SRAM cell and junction transistor stacking primarily based SRAM cell.

Table I shows the delay of the PMOS based SRAM cells. The SRAM cells were implemented using Cadence Virtuoso at 45nm CMOS technology. The power supply provided is 1.2V. Width and lengths of the transistors are kept at default for the Gated VDD technique. The width in Transistor stacking is made half the default value. From the above table it is determined that Gated VDD dissipates lesser static power in comparison to 6T SRAM cell and transistor stacking SRAM cell. Stacking based SRAM cell has lesser delay when compared to Gated VDD and conventional 6T SRAM cell with PMOS access transistor.

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