Low Power Lector Based Frequency Divider in 45nm Technology

[1]Meghana R, [2]Dr Kiran V

[1]PG Student, [2]Associate Professor
Dept. Of Electronics and Communication Engineering
RV College of Engineering Bengaluru, Karnataka, India

***Abstract*: Deep submicron CMOS circuits are currently confronting a significant technological issue with power consumption. Because of the high transistor density, low voltage, and thinner oxide layer, leakage power considerably and quickly rises as process technology becomes more advanced. Sub-threshold leakage current increases in CMOS devices as channel length is scaled down. In this paper, three low-power architectures—LECTOR, GALEOR, and DRAIN GATING—are contrasted. This paper aims to give a thorough analysis and comparison of the above mentioned leakage power reduction techniques that have been used. The power consumption and propagation delay of the fundamental CMOS NAND gates using the low power techniques are compared. With no or little change in the critical route delay of the circuits as a whole, significant power savings are accomplished. A performance analysis is done on a D flip-flop that is made using the above mentioned low power techniques. It is found that LECTOR based low power technique is the most efficient architecture. A frequency divider circuit is built using the most efficient D-flip flop, which can split frequencies by 2, 4, and 8. Cadence Virtuoso is used for the design and analysis using 45nm technology.**

***Keywords*: Cadence Virtuoso, 45nm, CMOS, NAND, D-flip flop, Low power, LECTOR based, GALEOR based, DRAIN GATING based, frequency divider, power, propagation delay**

I. INTRODUCTION

Low power design is developing quickly and ingeniously as a result of the rise in popularity of portable devices and the requirement to restrict the power consumption of exceptionally high density VLSI processors. The power consumption of switching components is becoming comparable to leakage power consumption in many high performance systems. In battery-powered systems, high power consumption decreases battery life and has an impact on cooling costs and dependability. Low power design for battery-operated gadgets thus aims to increase battery life while meeting performance standards.

There are three basic sources of power dissipation in digital CMOS circuitry. Signal transfer is the cause of the first. The supply voltage squared determines the variation in power dissipation caused by transitions. Short circuit currents, which flow directly from the supply to the ground terminal, constitute the second cause of power dissipation when the n-sub network and p-sub network of a CMOS gate conduct simultaneously. When the input(s) to and therefore the outputs of a gate are not changing, leakage power dissipation—also referred to as static dissipation—occurs. It is the third source of power loss.

The dynamic power and leakage power equations are given as follows

Dynamic Power, $P_{dyn} = C_{load} V^2_{DD} f$ - (1)

Leakage Power, $P_{leakage} = V_{DD} I_{leakage}$ - (2)

Where the supply voltage is VDD, the clock frequency is f, and the total load capacitance is Cload.

Since the leakage power changes linearly with supply voltage and the dynamic power varies as the square of supply voltage, lowering supply voltage is the most efficient way to achieve low power performance. Lowering the supply voltage while retaining the threshold voltage at its current level, on the other hand, results in a considerable speed loss since doing so also lowers the gate drive voltage, which lengthens the delay.

To address delay deterioration, lower threshold voltage (Vt) is required. When the threshold voltage is lowered, the leakage current below the threshold grows exponentially. With additional reductions in supply voltage and threshold voltage, leakage power may become more powerful than dynamic switching power.

Therefore the primary focus of the low power approach has been source voltage scaling. Due to this, circuits now operate at source voltages below the threshold voltage. Leakage, a significant source of leakage power, and weak inversion current result from a transistor's sub-threshold action.

A fundamental component of sequential logic circuits is the flip flop. It is a circuit that can store one bit of state information and has two stable states. When signals are supplied to one or more control inputs, the output changes state. The fundamental D Flip Flop contains outputs Q and Q as well as D (data) and Clock inputs (the inverse of Q). The PR (Preset) and CLR (Clear) control inputs are optional additions.

To split and decrease the frequency of a high frequency signal to obtain a lower frequency signal, a frequency divider circuit is employed. The frequency of the subsequent main clock pulses in a D flip flop decreases if the Q output is linked directly to the D input, providing closed loop "feedback" to the device.

This paper aims to give a thorough analysis and comparison of three low power techniques – LECTOR, GALEOR and DRAIN GATING based architectures [1]. The power consumption and propagation delay of simple CMOS NAND gates using low power techniques are compared. Performance investigation is carried out on a d flip-flop built using the aforementioned low power techniques. The most efficient architecture is found to be an LECTOR-based low power strategy. A frequency divider circuit that can split frequencies by 2, 4, and 8 is built using the best D-flip flop.

II. METHODOLOGY

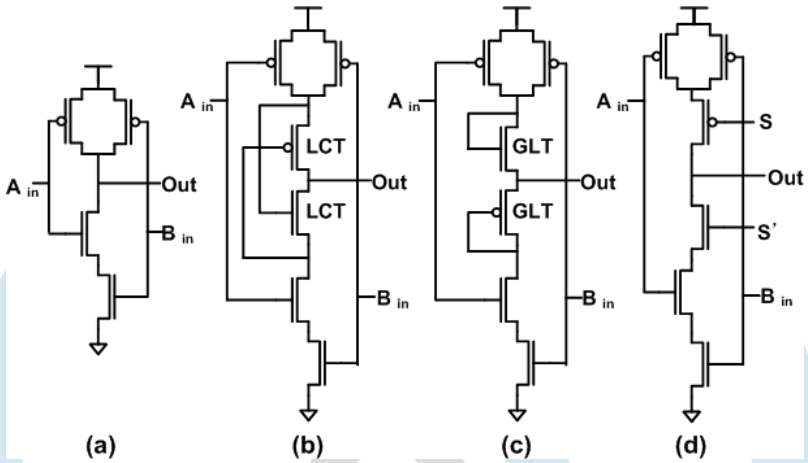

Figure 1. (a) Original Two-input NAND Gate (b) LECTOR NAND Gate (c) GALEOR NAND Gate (d) Drain Gating NAND Gate . [1]

Conventional CMOS 2 input NAND gate is shown in Fig 1(a).

LECTOR, which employs two additional transistors termed leakage control transistors (LCTs) put in series between the pull-up network and pull-down network in each CMOS gate, is one method of reducing leakage power. This method is shown in Fig. 1(b). Since one of the leakage control transistors is continually in close proximity to its cutoff zone, leakage current is reduced as a result of the route from Vdd to ground being more resistive.

Similar to the LECTOR method, as seen in Figure 1(c), the GALEOR approach moves the placements of additional transistors known as Gated Leakage Transistors (GLTs). The NMOS GLT is positioned between the pull-up network and the output, while the PMOS GLT is positioned between the pull-down network and the output. The lower output voltage swing is a problem for the GALEOR method.

As part of the drain gating strategy, additional sleep transistors are put in between the pull-up and pull-down networks to reduce leakage current. In Fig. 1 (d), the pull-up network and the network output are each coupled to a sleep transistor (S) for PMOS and a sleep transistor (S') for NMOS, respectively. When the system is in active mode, both sleep transistors are turned on in order to reduce the resistance of conducting lines and prevent performance deterioration. By increasing the resistance of the connection between the power supply and ground, the stacking effect, which occurs when both sleep transistors are turned off while the device is in standby mode, reduces leakage current. This method calls for an extra control input.

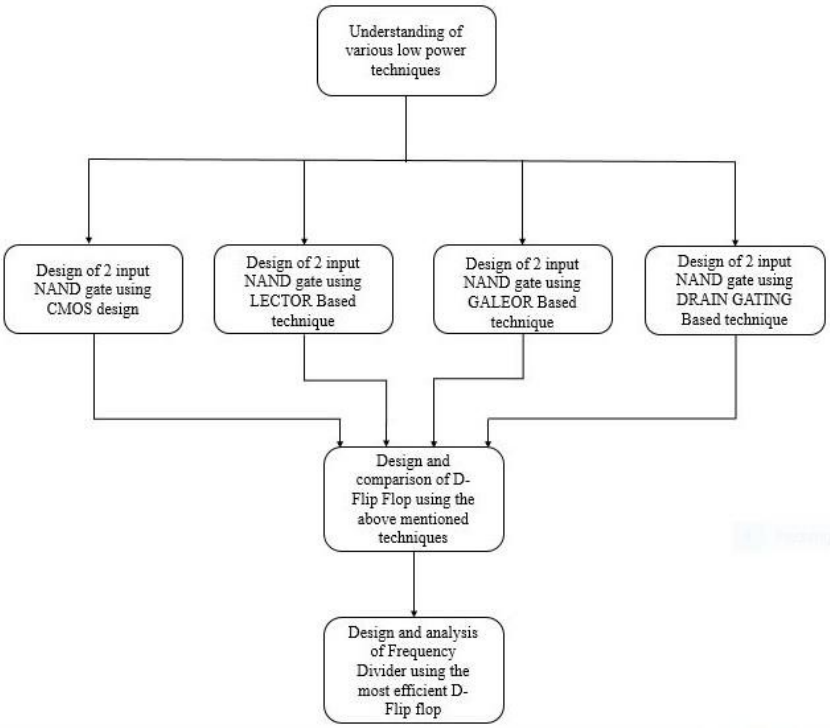

Figure 2. Design Methodology Flow

III. SCHEMATIC AND SIMULATION OF D FLIP-FLOPS

Two input NAND gates are designed utilizing conventional CMOS, low power LECTOR-based, GALEOR-based, and drain gating approaches after understanding the different low power methodologies. D-flip flops can also be designed using the corresponding NAND gates. The schematic of D-flip flop using NAND gates is shown in Fig.3

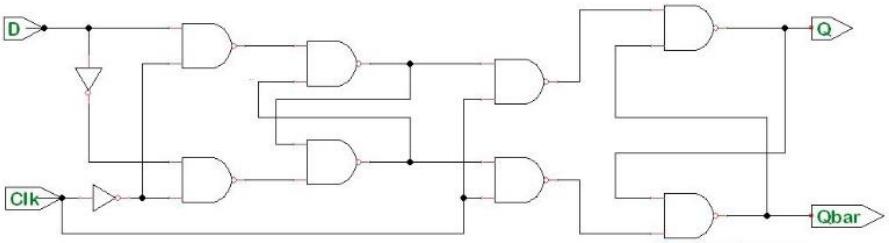

Figure 3. Schematic of D-flip flop using NAND gates

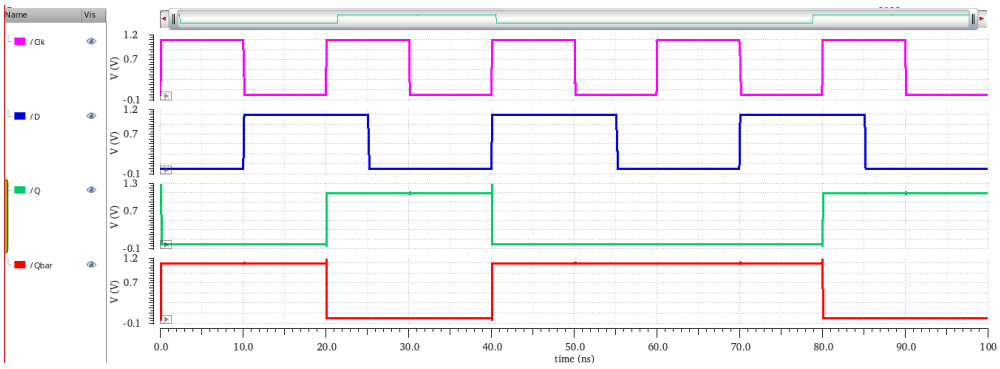

Figure 4. Transient Analysis of D-flip flop using conventional CMOS NAND gates

Figure 4 shows the output of a D flip flop. When the clock is high, the output Q is same as that of the input D. When the clock turns low, the previous state of the Q output is retained. Qbar is the complemented output of Q.

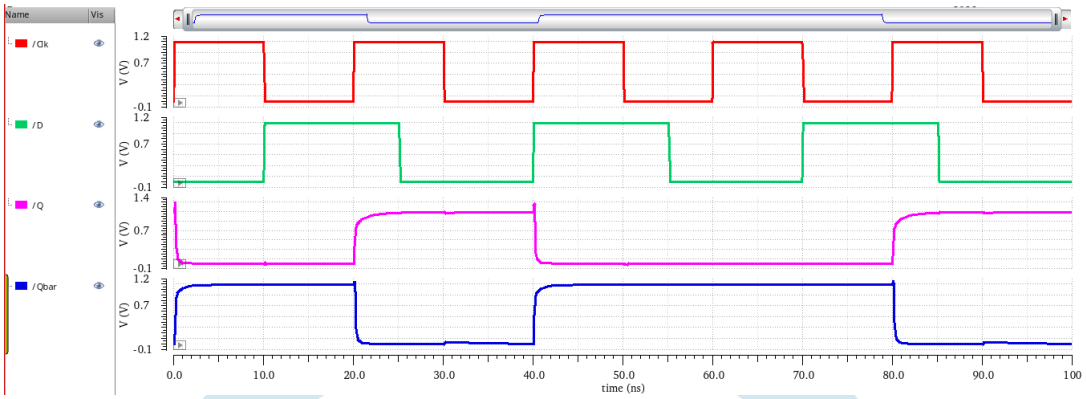

Figure 5. Transient Analysis of D-flip flop using LECTOR based NAND gates

Figure 5 shows the output of a D flip flop. The NAND gates that are used are designed using LECTOR based approach. The working of the D flip flop remains the same as mentioned in Figure 4. A slight delay can be observed in the outputs Q and Qbar.

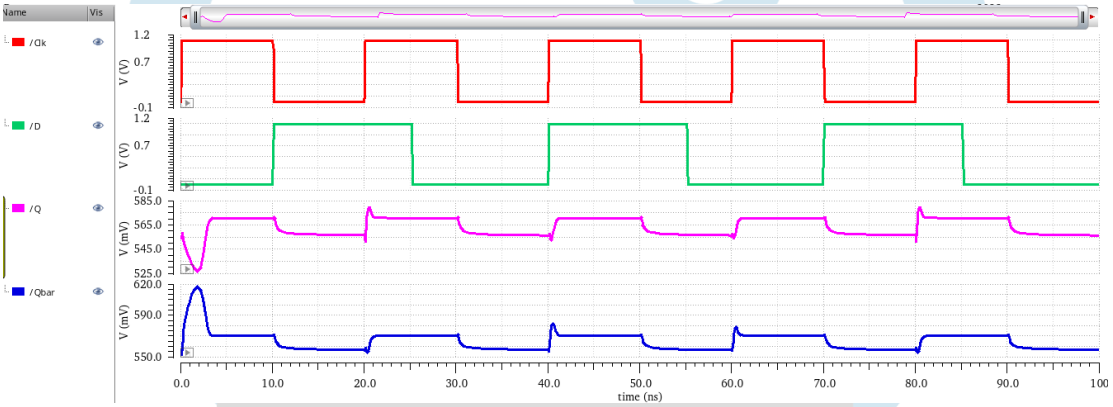

Figure 6. Transient Analysis of D-flip flop using GALEOR based NAND gates

Figure 6 shows the output of a D flip flop. The NAND gates that are used are designed using GALEOR based approach. The working of the D flip flop remains the same as mentioned in Figure 4. The degradation of the output voltage swing can be observed in the both Q and Qbar outputs.

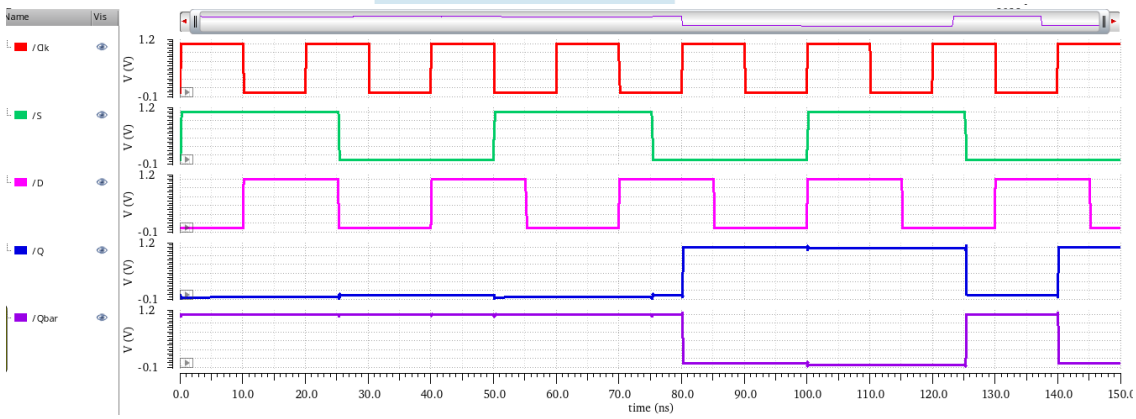

Figure 7. Transient Analysis of D-flip flop using DRAIN GATING based NAND gates

Figure 7 shows the output of a D flip flop. The NAND gates that are used are designed using DRAIN GATING based approach. An addition control input S is required for this design approach. The NAND gates performs its operation only when the control input S is 0, since S is connected to the PMOS and the complement of S is connected to the NMOS as shown in Figure 1(d).

The waveforms of D-flip flops using NAND gates designed using the various low power techniques can be seen in Figures 4, 5, 6 and 7. The degradation in the output voltage swing in GALEOR based technique can be observed in Fig 6. An additional control input S is required for DRAIN GATING based technique can be seen in Figure 7.

IV. SCHEMATIC OF FREQUENCY DIVIDER

The most efficient D-flip flop is used to build a frequency divider circuit. Three D-flip flips are used to achieve the divide by 2, divide by 4, and divide by 8 frequencies. This is depicted in Figure 8.

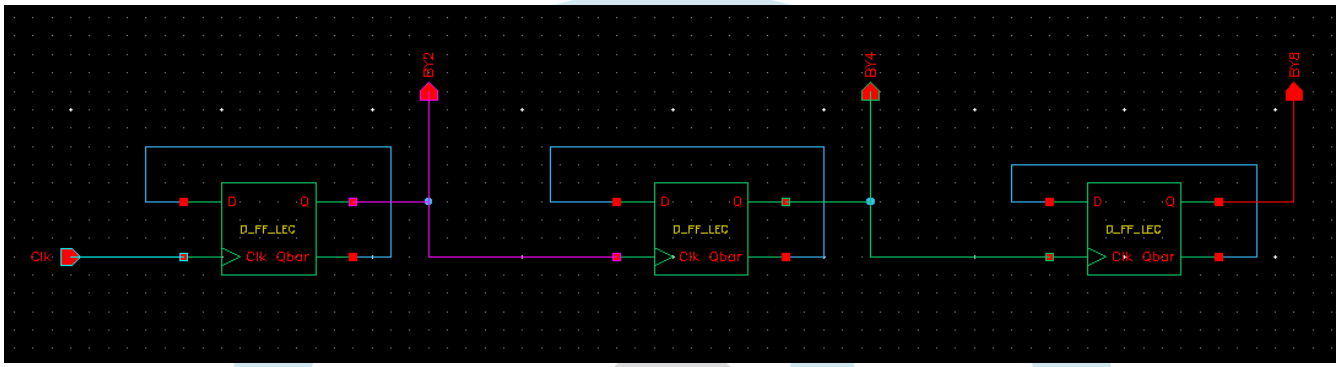

Figure 8. Schematic of frequency divider using D-flip flops

Figure 8 shows the schematic of a frequency divider that is designed using D-flip flops. The output is proved as a feedback to the D input of the flip-flop which helps in the reduction of frequency of the main clock. Using a single flip-flop provides a reduction of frequency by 2. In this work, 3 D flip-flops are used, and all the three division (divide by 2, divide by 4 and divide by 8) are observed.

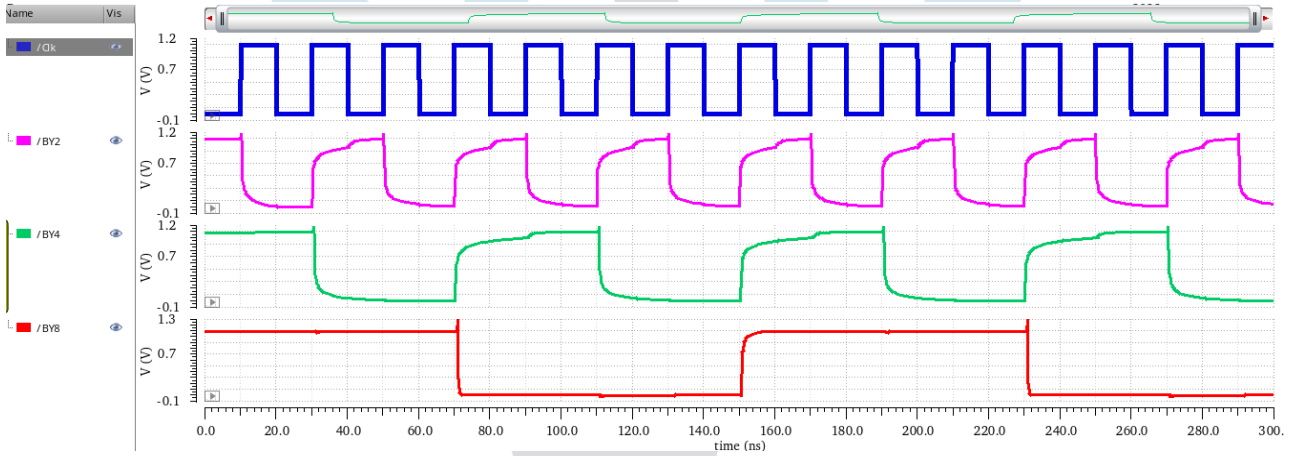

Figure 9. Transient analysis of frequency divider using D-flip flops

Figure 9 shows the output of the frequency divider. The division of frequencies can be observed in the waveform.

V. RESULTS

The power and propagation delays of D-flip flops developed using various low power techniques are compared. This can be seen in Fig 10 and 11 respectively.

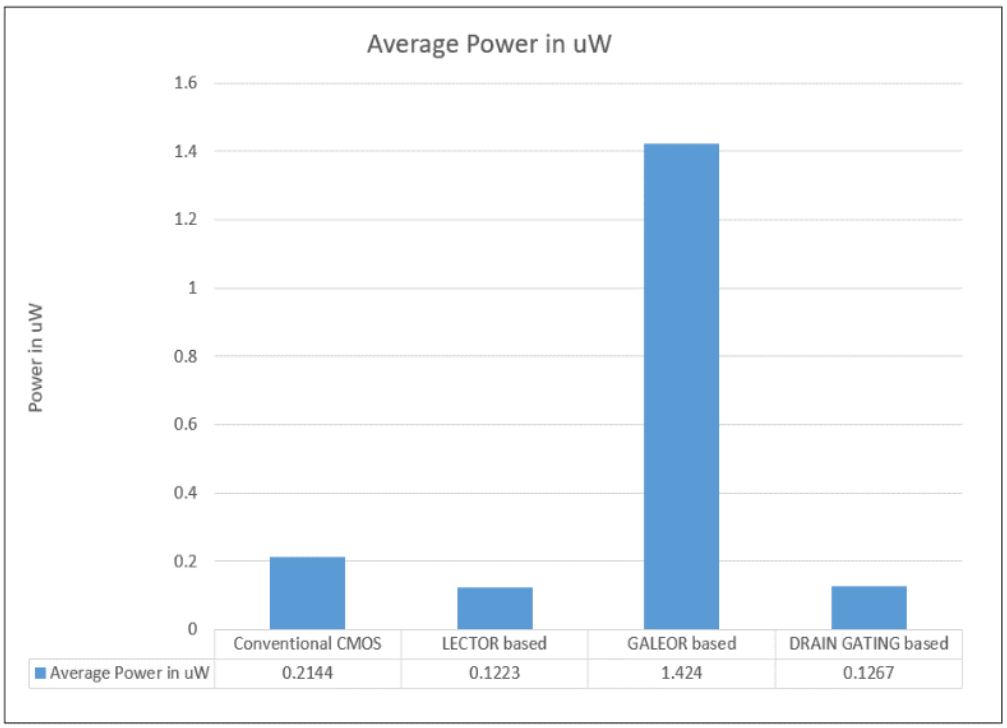

Figure 10. Average Power comparison

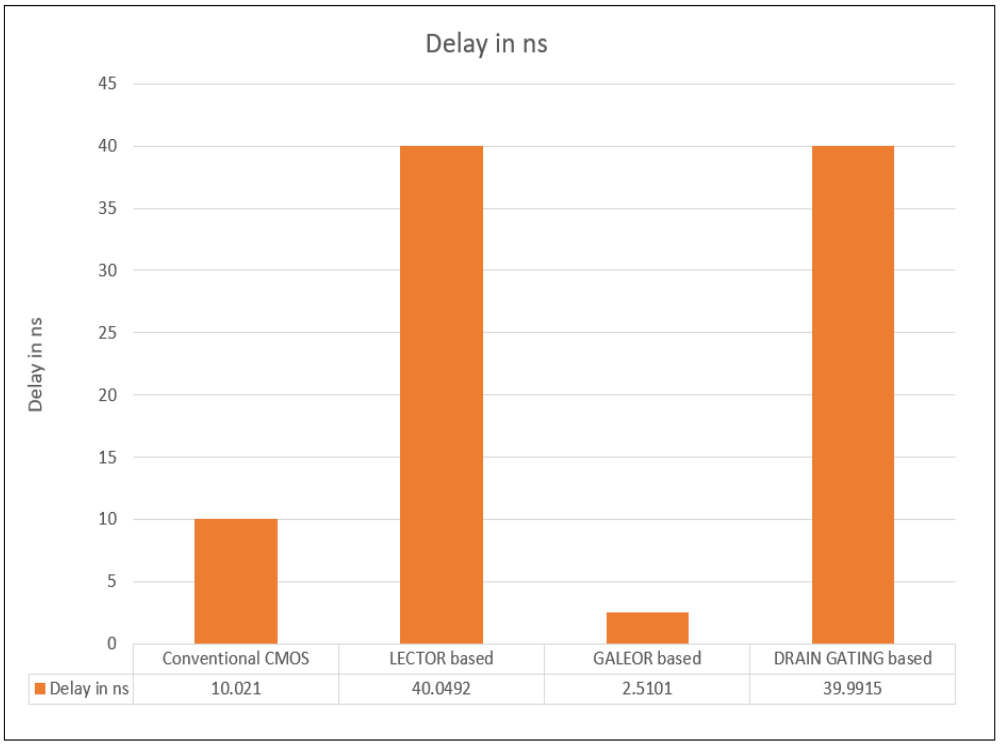

Figure 11. Propagation delay comparison

The performance analysis of frequency divider circuit is shown in the table below

Table 01. Performance Analysis of Frequency Divider

Parameter	Value
Average Power	476.7nW
Delay	140.723ns
Main Clock Frequency	50MHz
Divide by 2 Frequency	25MHz
Divide by 4 Frequency	12.5MHz
Divide by 8 Frequency	6.25MHz

VI. CONCLUSION

It can be observed that GALEOR-based technology uses the most power while experiencing the least delay. The reduced output voltage swing is another drawback of the GALEOR-based approach. The propagation delay and power consumption of LECTOR-based and DRAIN GATING-based approaches are nearly same, however the disadvantage of DRAIN GATING-based technique is that it needs an extra control input S, as was already discussed. The frequency divider circuit is designed utilizing the best low power approach, which is LECTOR based.

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