Design and Comparative Analysis of 4-Bit RCA for Low Power Applications

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***Abstract*: The active development in the domain of micro-electronic devices, led the need for the designs with high speed, low power dissipation, lower area and urge for several research intentions. There are several design techniques that are available which can be used for the circuit implementation in VLSI design, but a very few design configurations give the optimality at required satisfactory level. This work is keenly focused on reducing the values of delay, power and improve the stability of a 4bit RCA (Ripple Carry Adder), inducing various full adder design techniques.**
To increase battery life, data from comparative analyses of power, delay, and stability employing complementary metal oxide semiconductors, static energy recovery full adders, full swing gate diffused input, and different transistor counts are implemented. As an advancement to this work, new GDI design technique is implemented and found to be with respect to power, area and delay values in comparison with existing traditional techniques. The Cadence Virtuoso tool with 45nm CMOS technology is used to simulate Power and delay. The results shown an improved performance for the suggested design at a supply voltage of 1.0V in terms of power and latency. According to simulation results, the proposed design shows the least power consumption and a fewer delay than other full adder circuits already in use. As a result, the PDP is enhanced in comparison to other full adder designs.

***Keywords*: CMOS, SERF, GDI, FS-GDI, Full Adders, PTL, Short Channel Effects.**

I. INTRODUCTION

In earlier days, VLSI design applications were focused mainly on area, cost and reliability rather than power. The advancements in the modern technologies and the designs such as mobile phones, laptops with the multi-core designs and micro-electronics led the way for advancements in the field of research and have been a goal to accomplish better design. The drawback of portable devices was, unreliable power supply due to high power consumption which affects battery life and may cause serious damage in silicon parts of the devices. It requires huge packaging cost with advanced heat dissipating designs with less power consumption. Manufacturing of these designs with low power techniques will draw an additional impact on the existing fabricating technologies and require additional research in fabrication process. Adapting different optimization techniques at architectural, algorithmic, gate or circuit-level designs will help in reducing the power dissipation and with optimality in the delay of the designs. Here, we focus on transistor-level power optimization. Numerous adder circuits with various numbers of transistors have been designed using full adders. The implementation of various 1-bit and 4-bit full adder designs 28-T CMOS design, 10T GDI style design, 10T SERF design, and 16T FS-GDI technique as well as comparative analysis of those designs are done in this article.

II.METHODOLOGY

1. Basic Full Adder design:

A 1-bit Full adder circuit has 3 inputs named A, B, & Cin. A cascade of adders that adds binary integers typically includes the Full adder as one of its parts. The Block diagram representation is shown in Fig 1. The outputs of the full adder are sum and carry out. Two EX-OR gates, two AND gates, and one OR gate can be used to build the 1-bit CMOS full adder. The logic equation for SUM and Carry output are

$$\text{Sum} = (A \text{ xor } B \text{ xor } C_{in})$$
$$\text{Carry} = (A \text{ and } B) \text{ or } (B \text{ and } Cin) \text{ or } (A \text{ and } C_{in})$$

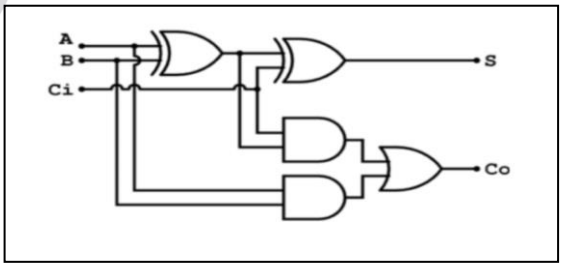

Fig 1: Circuit diagram of full adder

2. Overview of GDI:

The GDI cell, which contains just two transistors and a structure resembling a conventional CMOS inverter, initially looks to be a typical CMOS inverter. Fig. 2 depicts the design of a GDI logic cell. However, a GDI cell has three inputs: P, the source input for

pMOS, G, the common gate input for both nMOS and pMOS, and N, the source input for nMOS. Numerous Boolean functions are implemented by a simple GDI logic cell and shown in Table1. This depends on a change in the input configuration of the GDI cell. In Static CMOS logic, the implementation of the majority of these functions is more complicated and necessitates 6 to 12 transistors; however, with GDI cells, it is far more efficient (just 2 transistors are required). The Multiplexer (MUX) is the most intricate Boolean logic that can be built with a simple GDI cell and has been shown to be more effective than CMOS in representing logic.

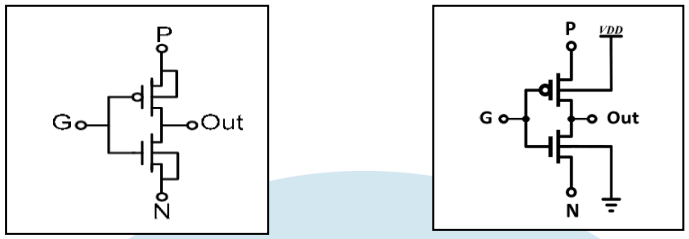

Fig 2: Circuit diagram of basic GDI and M-GDI logic cells.

N	P	G	OUT	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B$+AC	MUX
0	1	A	$\overline{A}$	NOT

Table-1 Implementation of Boolean function with a simple GDI logic cell.

Threshold voltage decreases in GDI gates limit current drive, which impairs the gate's functionality. The full swing of the output voltage gets affected when the designs are cascaded in series for building complex design structures. By combining a multiple V_{TH} method with swing-restoration buffers, these impacts can be considerably diminished. According to this method, low threshold transistors should be used in any path where a voltage drop is anticipated. By doing this, there will be little voltage drop at the output. Additionally, high threshold transistors are used to create all regenerative inverters. The direct-path static power in the inverters is reduced as a result of this arrangement. The majority of static digital designs used today are built using CMOS NAND and NOR gates. NAND and NOR gates can be built with just 4 transistors, and each of these function as a universal set, which is one of the reasons behind this. The GDI approach, which is particularly effective for the development of different gates, including MUX, AND and OR (see Table1), uses about the same number of transistors for the implementation of NAND/NOR gates as traditional CMOS technique.

3. Overview of FS-GDI:

The main issue encountered while using a GDI technique is drop over the full swing of an output. This would reduce the noise margin of a design. The proposed design using modified GDI uses three more transistors, that would restore the output to full swing. Full Swing GDI technique focus on attaining full swing at each gate designed. The output swing can be achieved at an expense of increase in number of transistors, area and power, but when compared with respect to CMOS and PTL implementations FS GDI uses lesser number of transistors, hence results in reduced area and power values. The design of few logic gates using FS GDI is as shown in the fig 1.4

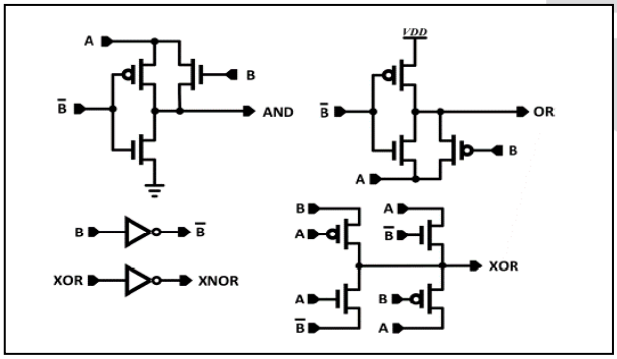

Fig 3: Logic gates using FS-GDI

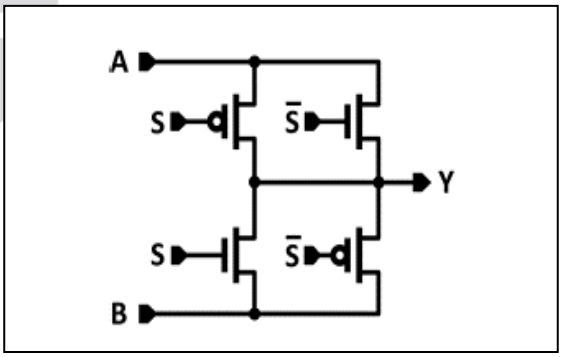

Fig 4: Mux using FS-GDI

III. DESIGN

1. Design of 28-T CMOS Full Adder:

A CMOS consists of pMOS stacked upon nMOS transistor acting as an inverter in its behavior. Pull-up transistors are known to produce a strong-one and pull-down transistors a weak-zero. Several CMOS architectures were used to estimate the average power dissipation. The pull-up and pull-down transistors used in the 28T design result in full swing outcomes and improved driving capacities. The primary flaw of this design is the increased transistor count. As a result, input capacitances, increase in latency, and the value of dynamic power consumption all rise. Figure 5 displays the architecture.

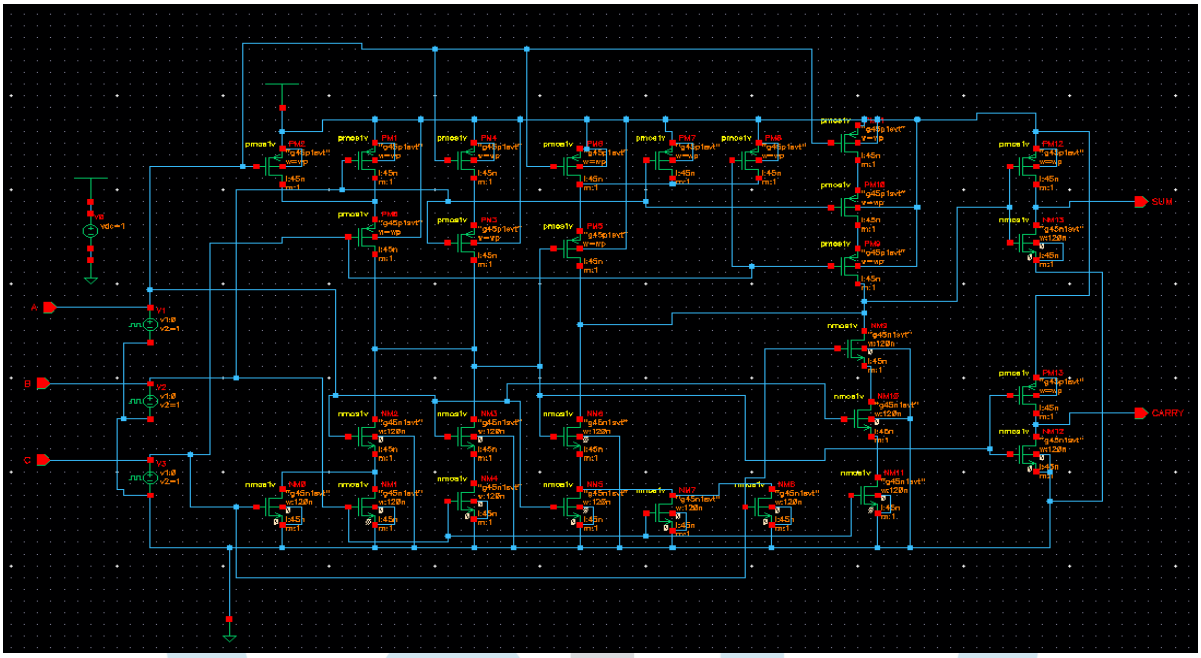

Fig 5: Circuit of 28T CMOS Full-Adder

2. Design of 10-T SERF 1-bit Full Adder:

Implementing the XOR and XNOR gates and balancing the output gate delays are done using SERF logic design. The short circuit power has been reduced by employing this design because there is no direct connection from VDD to ground. Therefore, the charge in the load capacitance gets reused by the control gates. Although this arrangement is effective at storing energy, there are several drawbacks. The internal node power supply fails as a result it would impact output nodes' full swings. There could be threshold issues with this cascaded power supply that appear throughout the design architecture. The block diagram is shown in figure 6.

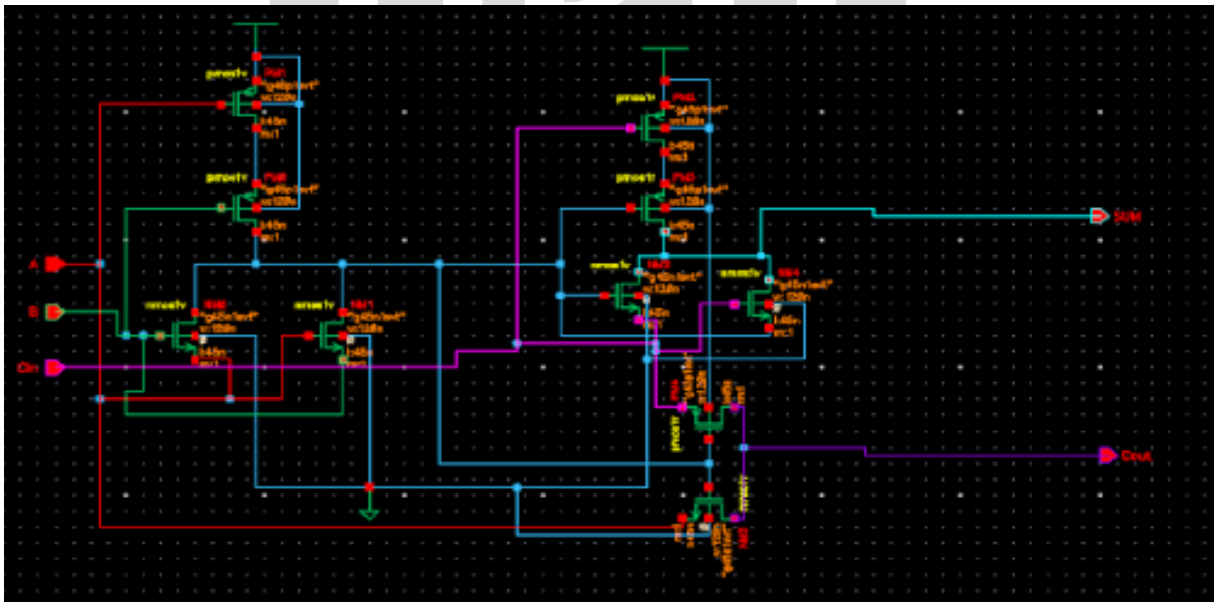

Fig 6: Schematic of 1bit Full Adder using 10T SERF

3. 10T GDI Full Adder Design:

The circuit's primary building blocks are multiplexors, XORs, and XNORs. There are two multiplexors at the output. Mux1 with XOR logic yields the output sum, while mux2 with XNOR logic yields the carry output. The delay is lower in this case because there is just one mux in the line of carry propagation. The structure is shown in figure 7.

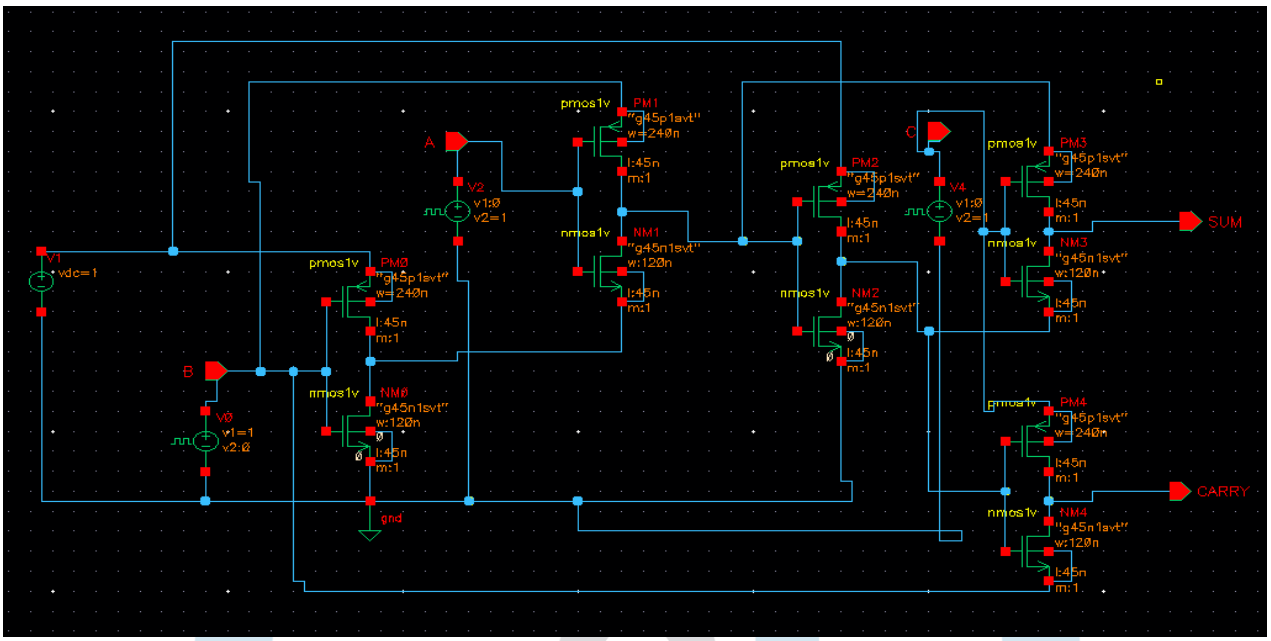

Fig 7: Schematic of 1bit Full Adder using 10T GDI

4. Proposed design for 10T GDI Full adder:

To increase the output swing, the proposed design makes use of full swing restoration (SR) transistor. The full swing restoration (SR) transistor includes either nMOS or pMOS with one inverter. Only when the threshold drops at the output does this swing restoration transistor come on. As only one of the logical levels (VTH instead of 0 V or VDD-VTH instead of VDD) can experience an output threshold decrease, just one swing restoration transistor is needed to ensure full swing operation. The swing restoring transistor can be controlled when the gate input signal of the SERF cell is represented are inverted in the circuit. The proposed design is shown in figure 8 and the simulations are shown in figure 12.

$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B})$$

$$CARYY = (\overline{A \oplus B})B + (A \oplus B)C$$

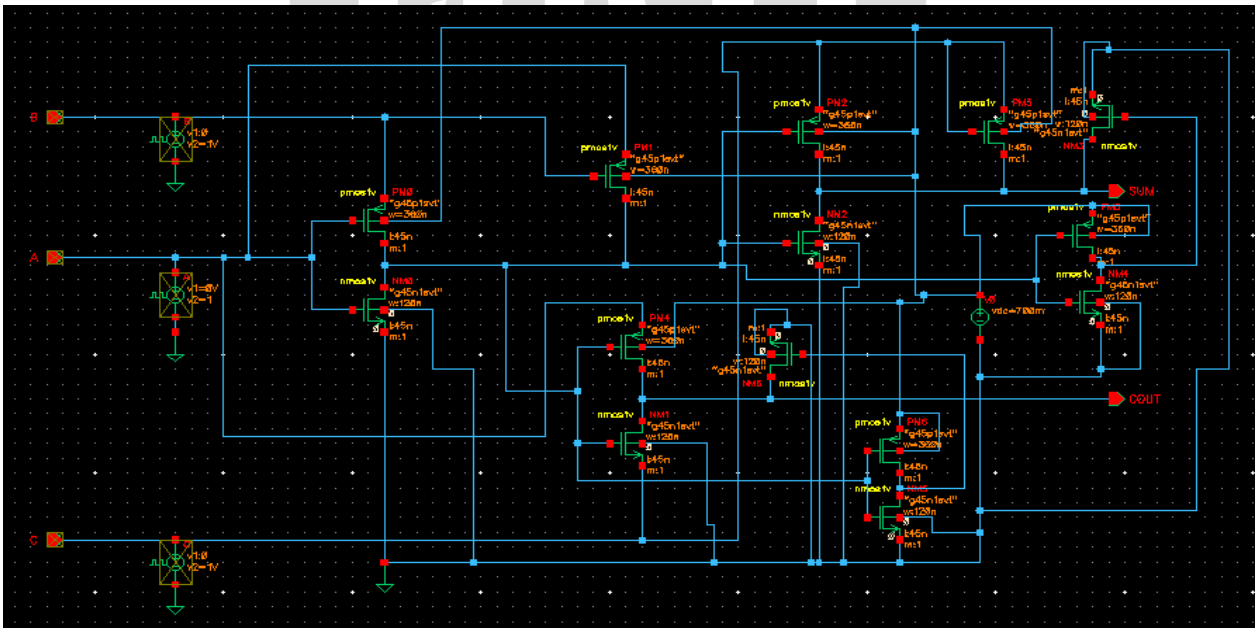

Fig 8: Schematic of proposed 10T GDI Full Adder

5. Full adder design using FS-GDI technique:

The FS-GDI technique focus on achieving the full swing over the output voltage at gate level. The schematics of basic logic cells as shown in fig 3 and fig 4 are used for designing a one-bit full adder with more stable output levels.

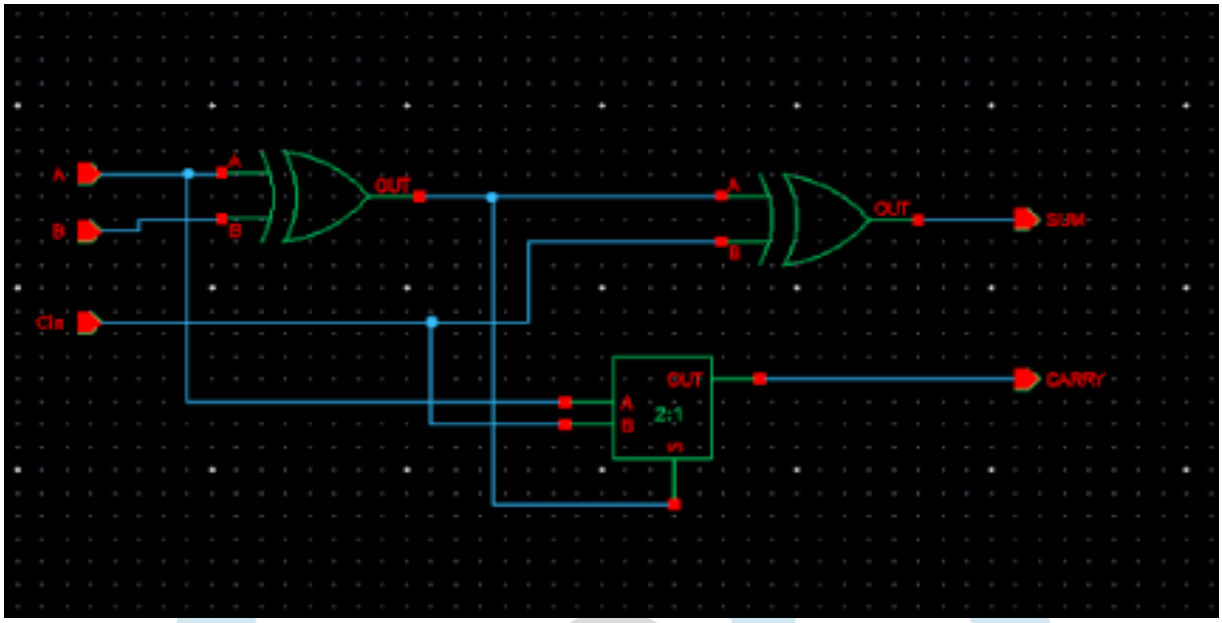

Fig 9: Schematic of 1-bit Full Adder using FS-GDI logic

6. Design of RCA using the above design logics:

RCA is a combinational logic circuit that can be used to perform addition operation on two different numbers. A N-bit RCA requires N adders to add two different numbers of N-bit each. The schematic of 4-bit RCA is shown in the fig below. All the logic designs which are discussed above are used to develop RCA and the designs are compared for delay, power and PDP.

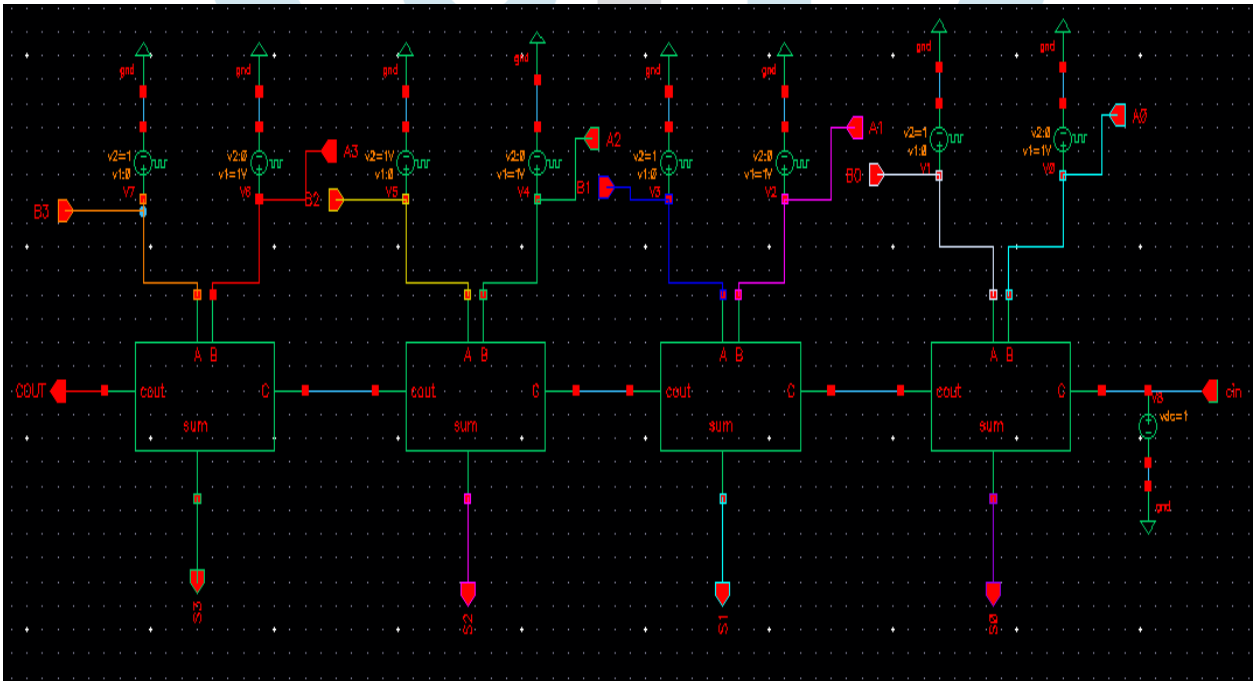

Fig 10: Schematic of 1-bit Full Adder using FS-GDI logic

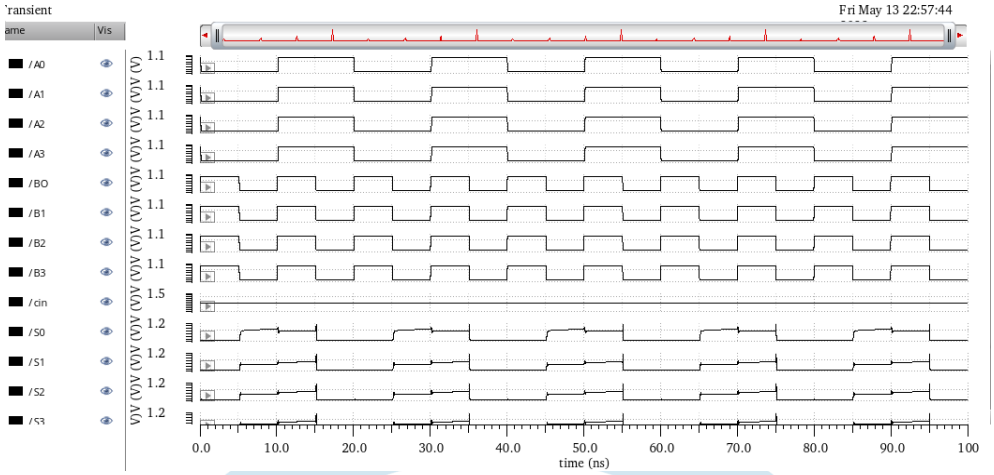

Fig 11: Simulation waveform of 4bit RCA using 1bit proposed GDI based Full adder

Fig 12: Simulation waveform for 1bit proposed GDI based Full adder

IV. RESULTS AND ANALYSIS:

The performance of any design is determined with respect to delay, transistors count, and power consumption. Using 45nm technology for 1bit and 4bit Ripple carry adder are designed. Comparing the GDI, FS-GDI, and CMOS-based full adders in terms of average power, transistor count, and delay is done. The results of the GDI-logic based full adder design are significantly better than the CMOS-based full adder in terms of power consumption and decreased delay by neglecting voltage swing, as can be shown from table 1. The work is carried out with 1-bit and 4-bit designs. The proposed design gives much better results.

Table-2. Comparison of a 1bit full adder using 45nm technology.

DESIGNS	CMOS	SERF	GDI	FS-GDI	PROPOSED DESIGN FOR GDI
DELAY	108.3ps	61.19ps	57.326ps	43.43ps	40.2ps
POWER	702nW	181.6nW	156.2nW	131.03nW	165nW
PDP	$7.62*10^{-17}$J	$1.147*10^{-17}$J	$0.894*10^{-17}$J	$0.56906*10^{-17}$J	$0.6624*10^{-17}$J
TRANSISTOR COUNT	28	10	10	18	14

Table-3. Performance Comparison of a 4bit RCA using 45nm technology.

DESIGNS	CMOS	SERF	GDI	FS-GDI	PROPOSED DESIGN FOR GDI
DELAY	324.9ps	183.57ps	171.978ps	221.06ps	120.6ps
POWER	2.106uW	430.5nW	308.6nW	513nW	495nW
PDP	$6.8423*10^{-16}$J	$7.902*10^{-17}$J	$5.3686*10^{-17}$J	$11.34037*10^{-17}$J	$5.969*10^{-17}$J
TRANSISTOR COUNT	112	40	40	72	56

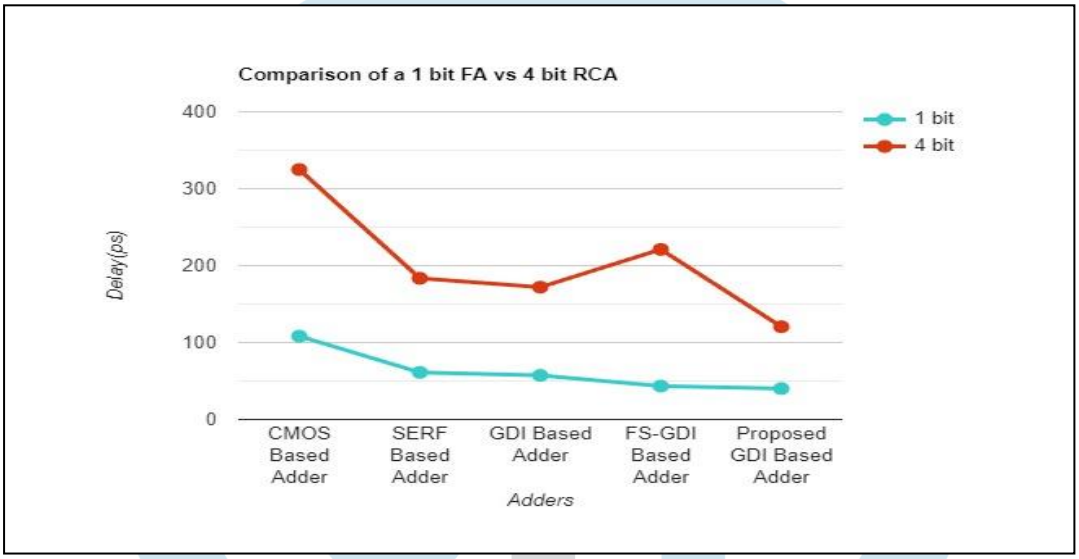

Fig 13: Graphical analysis of delay values obtained for 1-bit FA and 4-bit RCA for different low power techniques

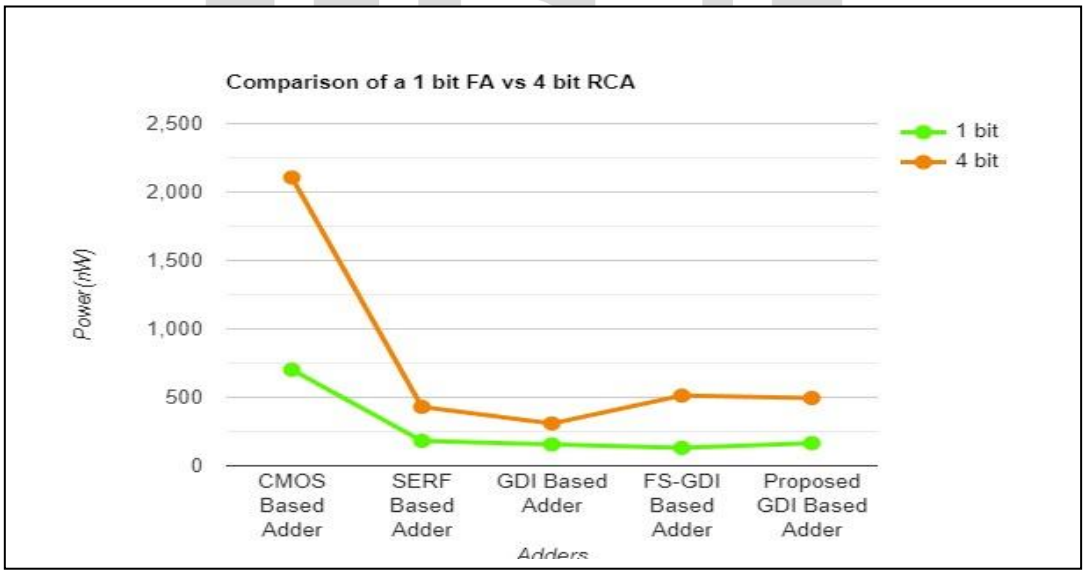

Fig 14: Graphical analysis of power dissipation for 1-bit FA and 4-bit RCA for different low power techniques

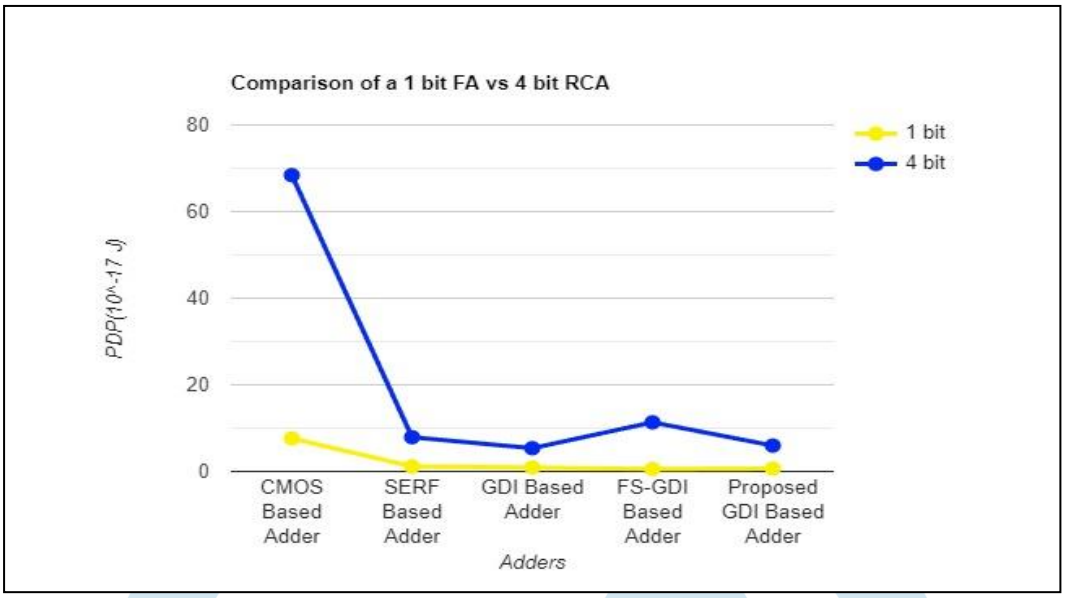

Fig 15: Graphical analysis of PDP for 1-bit FA and 4-bit RCA for different low power techniques

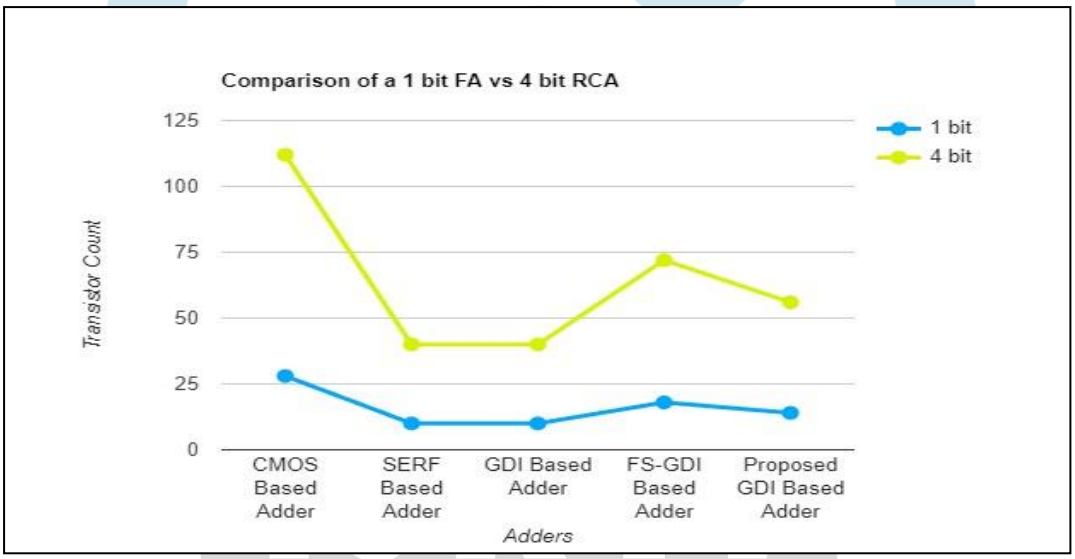

Fig 16: Graphical analysis of transistor count for 1-bit FA and 4-bit RCA designed with different low power techniques

V. CONCLUSION:

From the obtained simulation results, the comparison of average power, transistors count, and delay between the GDI, FS-GDI and CMOS-based 1bit and 4bit Ripple carry adders is done. Results of the GDI-based full adder are found to be optimal than the CMOS-based full adder in terms of power consumption and reduced delay by neglecting voltage swing. It is observed that the proposed design not only boosts the voltage swing but also consumes the least power and least delay compared to the CMOS-based full adder design. This in turn improves the PDP compared to other full adder circuits. Hence the proposed full adder circuit can be used for low power and high-speed application.

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