Design for SIMD MAC Unit Using 2-Bit Adders and Multipliers

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***Abstract*: The advent of digital circuits made it easy to realize many mathematical operations using the binary Boolean functions. The only problem was that, the mathematical operations were able to run at a significantly high speed with great accuracy for unsigned or signed integer numbers. Various architectures were able to accelerate the performance of mathematical operations on integers. But most of the real-world problems required operation with real numbers and hence either fixed point or more importantly floating-point arithmetic was necessary. It is possible to run different algorithms to execute operations on floating point numbers in an architecture designed for integer numbers. But the amount of CPU cycles required increases substantially with the complexity of problems involved, the precision required and accuracy as well.**

It is possible to develop architectures for fixed-point real numbers. But the reusability of the architecture is quite difficult for higher precision. For high accuracy or precision, the architecture hardware utilization increases exponentially. The conversion of fixed point to floating-point increases hardware as well. Hence, we have the IEEE 754 format for single/double precision floating-point architecture. But the amount of power spent and the hardware requirement is equally high. The time required to produce a stable output is quite high and the floating-point computation is the basic requirement in the overall algorithm of neural networks.

***keywords*: Mathematical operations, ALU, CPU,Vedic algorithm, Adders, Multipliers**

I. INTRODUCTION

The real-world signals we encounter are analog in nature. The primary communication with the external world is using analog signals. The use of digital signals arises due to various advantages among them being noise immunity and fast computation architectures and easy development of architectures. The architectures for digital computers or for any digital computation is for integer computation. The conventional procedure to compute floating-point arithmetic involved using the integer-based architecture with software support (algorithms). But the algorithms consumed large CPU cycles.

This reduced the throughput of the CPU. To increase the throughput, efficient algorithms have been developed, but the CPU cycle consumption reduction is quite feeble. The solution has always been to develop a complete floating-point unit separately operating on data or to develop floating-point architecture CPUs. The latter complexity is tremendous and hence, the former is preferred. The CPU off-loads floating-point arithmetic to this complete module. Hence, as a designer it is quite challenging to design a dedicated module for floating-point arithmetic which is highly efficient, low power, low area and is as fast as the ALU. The constraint of usage in real-time applications and further those involving human life require high precision facility for proper training. Although, this IEEE754 may be favorable for the case of training, the time and power consumed is significantly high. The computation of the same in a real-time application may not converge required results. Hence, the easier approach to achieve speed and power efficiency without much reduction in accuracy of the model is to use fixed-point arithmetic architectures. This reduces the hardware significantly and more importantly it's possible to obtain results for every clock cycle. This makes usage of this system architecture in real-time applications and possible optimization towards the application.

The IEEE 754 format for single/double precision floating-arithmetic facilitate an easy architecture based on the algorithm. The algorithm is a multi-cycle-based algorithm. The design takes multiple cycles to evaluate the output but consumes significantly lesser cycles compared to an integer-based architecture with software support. Today many processors and SoC use a floating-point compute unit separately. The architecture of this unit may involve multiple architectures supporting both fixed-point and IEEE standard floating-point as well. It has become necessary to use the design as a separate unit, so that it could be used by different modules or designs. In a modern SoC, there are different compute designs apart from the processor like DSP, Video encoder/decoder, security designs etc. Hence floating-point unit should be able to accommodate the necessary architectures to facilitate the usage by these other compute designs. It's possible to have both the IEEE 754 architecture and fixed-point compute unit together on a chip and software support can utilize both to achieve required application. But the fixed-point architecture reusability is extremely low. With the versatility of applications arising every day, it is required to have a new core logic which only processes for a AI application. These new lines of processors are called 'Neural processors. Their architecture consists of simple CPU core but the chip is majorly filled with compute units which accelerate the computations of the AI applications.

The major research happens to be in the amount of versatility that could be brought in these acceleration units. It is possible to modify the IEEE standard to user requirements and architecture. But this reduces the reusability of the design. This flexibility to modify the IEEE standard is helpful in easy design of architectures for DSP and other compute designs whereas the trade-off is the reusability and technical aspects like precision and accuracy and overall features of final product being developed.

II. METHODOLOGY

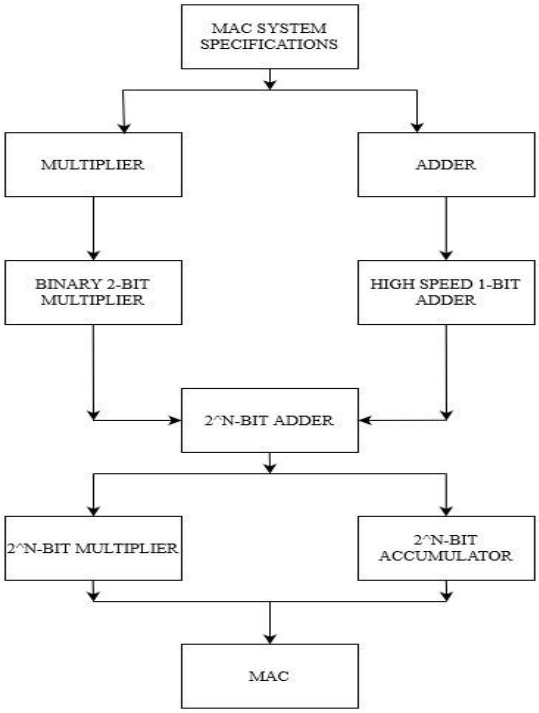


Fig 1: Flowchart for MAC design

The SIMD MAC architecture requires a basic MAC unit. The high-speed multiplier is designed based on Vedic algorithms, which 2-bit binary multipliers and higher order adders. The high-speed adder is designed using minimal transistors. This is necessary as the same adder is used in multiplier design. The 2-bit binary multiplier is designed using and gates and half-adders. The 2-bit binary multiplier is used in the design of a 4-bit vedic multiplier. Higher order multipliers are designed using the high-speed higher order adders. The basic cells required are inverter, AND gate, XOR gate. These basic cells are optimized for minimum delay, minimum area and equal rise and fall time. The half adder, 1-bit full adder are constructed using these basic cells. The 2-bit binary multiplier and higher order adders using 'RCA' architecture are constructed. The 2-bit binary multiplier and higher order adders are used to design higher order multiplier using vedic algorithm.

III. SCHEMATIC OF TG ADDER

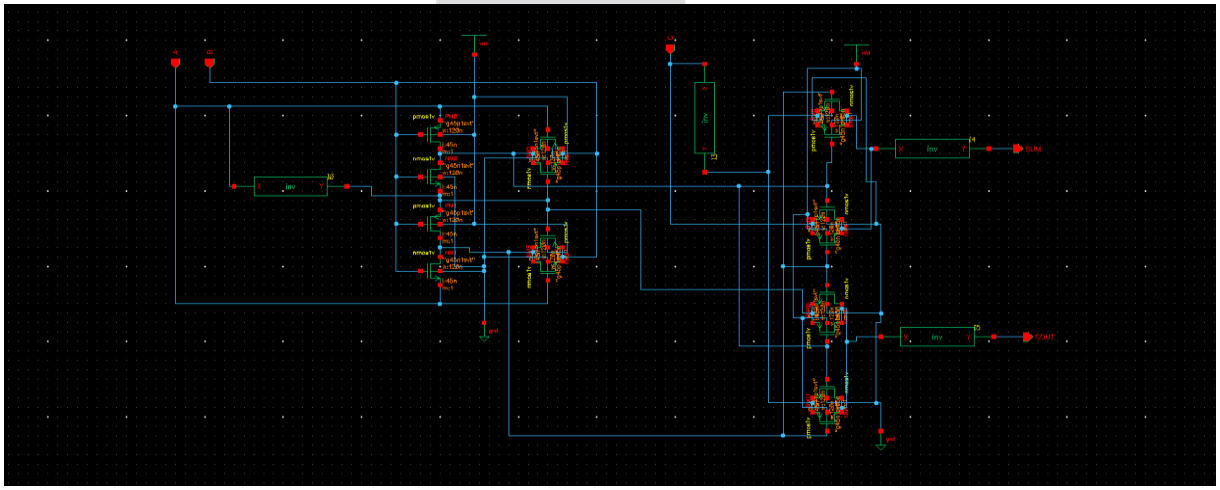


Fig 2: TG adder schematic

The Fig 2, represents the transmission gate 1-bit adder schematic. It uses a total of 24 transistors. The TG adder is sized for minimum delay. This minimum delay is obtained by converging the function for equal rise and fall time.

$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B})$$
$$CARYY = (\overline{A \oplus B})B + (A \oplus B)C$$

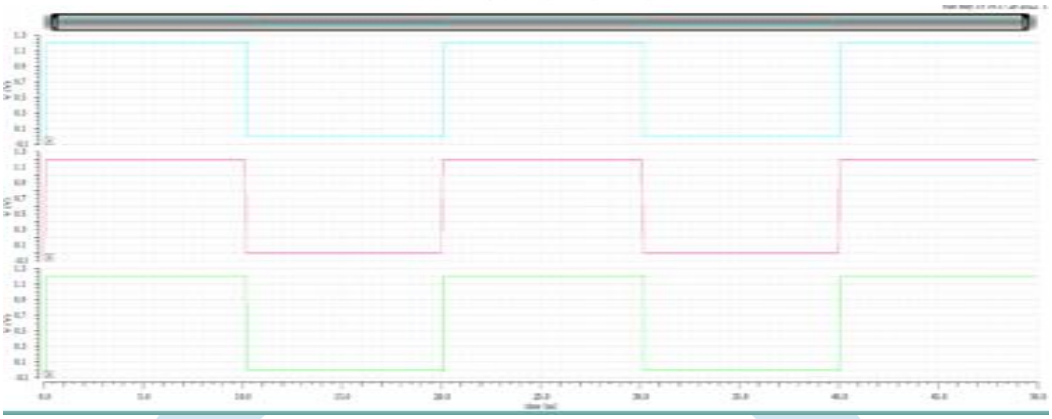


Fig 3: TG adder transient response

The Fig 3, represents the transient response of the TG adder. The delay for input to sum is **56.73ps**, the input to carry delay is **51.05ps**.

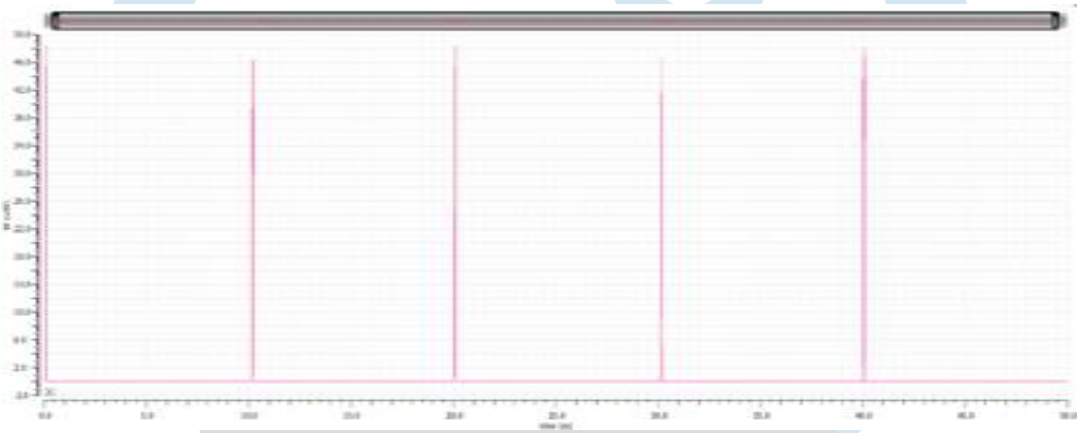


Fig 4: TG adder power consumption

The Fig 4, represents the power consumption of the TG adder. The total power consumption is **207.4nW**.

IV. SCHEMATIC OF CPL ADDER

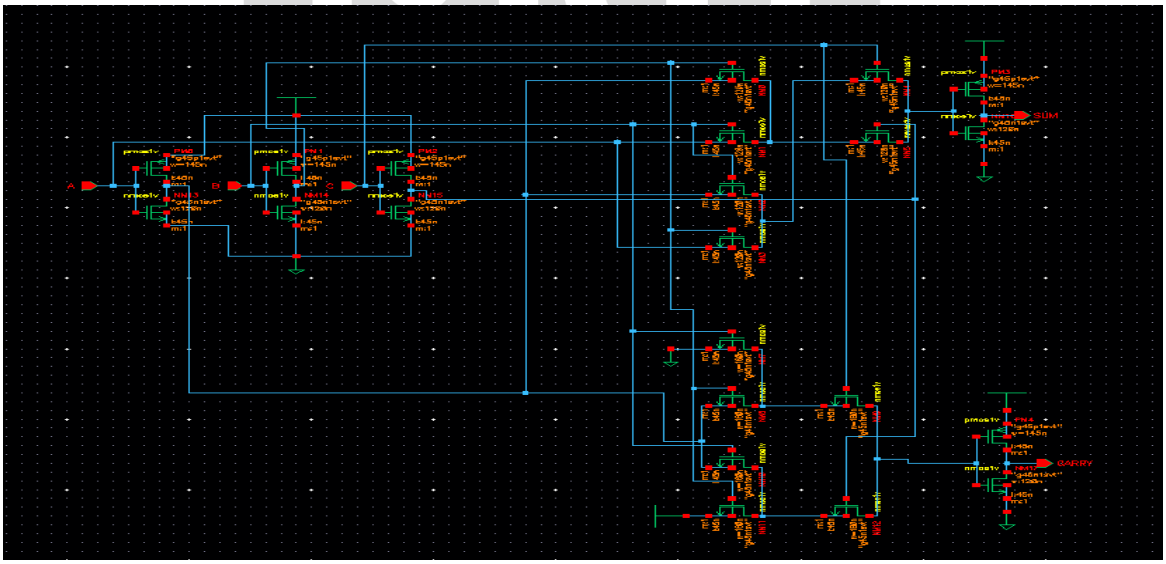


Fig 5: CPL adder schematic

The Fig 5, represents the Complimentary Pass Transistor (CPL) 1-bit adder schematic. It uses a total of 22 transistors. The CPL adder is sized for minimum delay. This minimum delay is obtained by converging the function for equal rise and fall time.

$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B})$$
$$CARYY = (\overline{A \oplus B})B + (A \oplus B)C$$

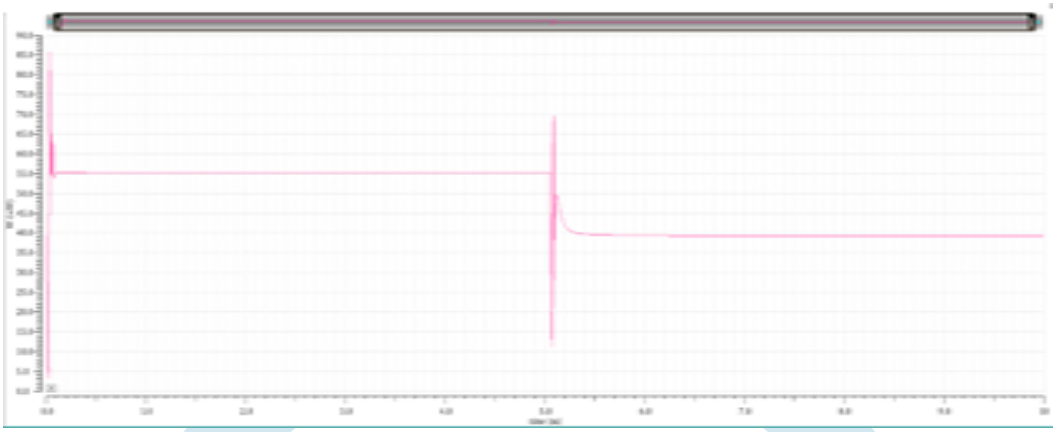


Fig 6: CPL adder power consumption

$$P_{total} = P_{dynamic} + P_{static}$$

The Fig 6, represents the power consumption of the CPL adder. The total power consumption is **47.42µW**.

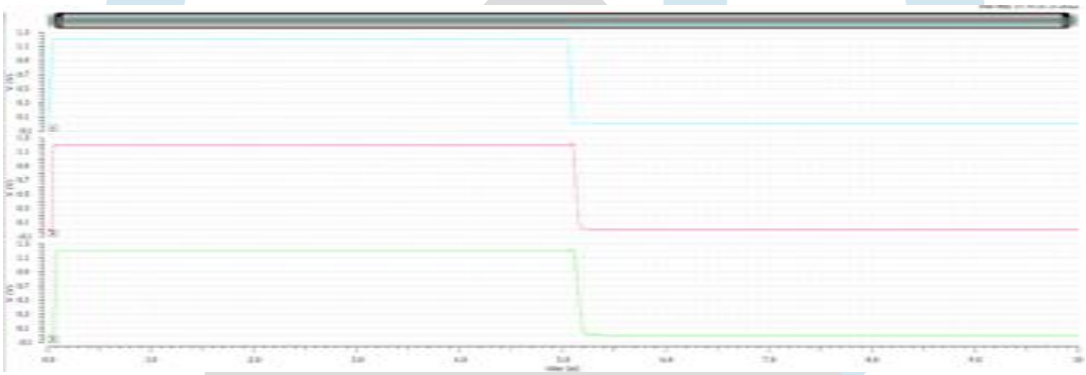
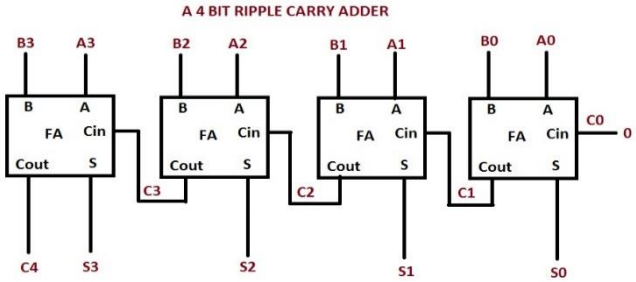


Fig 7: CPL adder transient response

The Fig 7, represents the transient response of the CPL adder. The delay from the input to the sum is **78ps** while the delay from the input to the carry is **57ps**.

V. SCHEMATIC OF 4 BIT RIPPLE CARRY ADDER



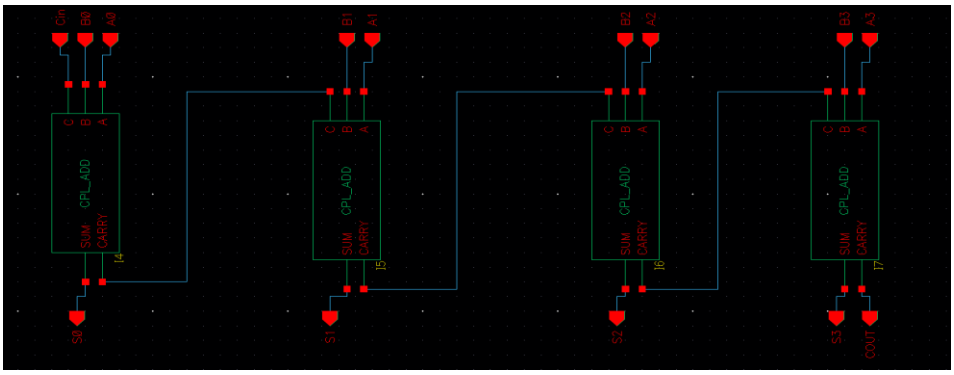


Fig 8: 4-bit ripple carry adder

The Fig 8, represents the schematic of 4-bit ripple carry adder either using CPL adder or TG adder. The adder is sized for minimum delay. This minimum delay is obtained by converging the function for equal rise and fall time.

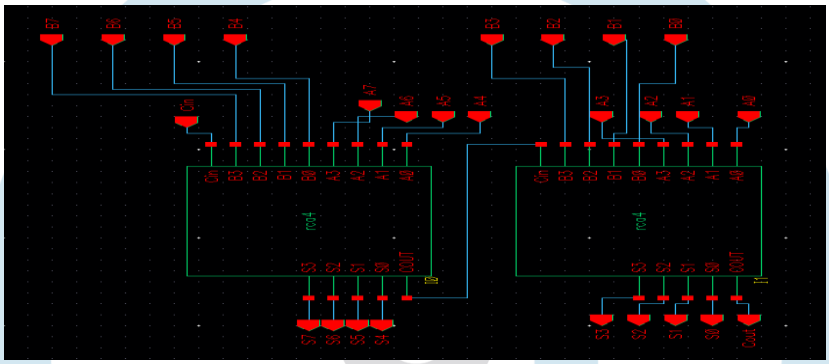


Fig 9: 8-bit Ripple Carry Adder (RCA) schematic

The Fig 9, represents the schematic of 8-bit ripple carry adder using 4-bit ripple carry adder. The adder is sized for minimum delay. This minimum delay is obtained by converging the function for equal rise and fall time.

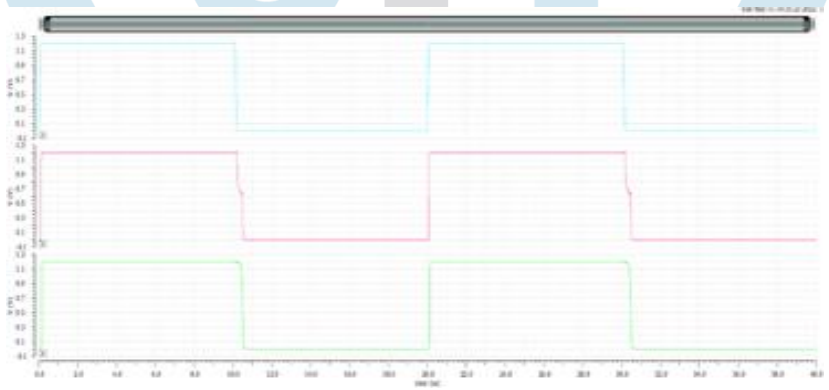


Fig 10: 8-bit RCA transient response

The Fig 10, represents the transient response of the 8-bit RCA. The delay from input to the sum is **337.6ps**, while the delay from the input to the carry is **323.4ps**.

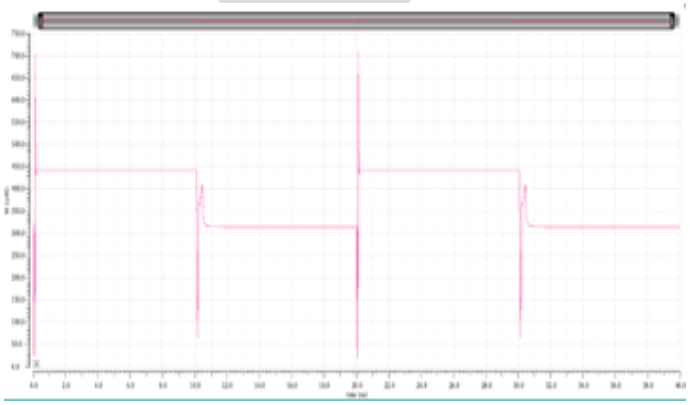


Fig 11: 8-bit RCA power consumption

Fig 11, represents the power consumption of the 8-bit RCA. The total power consumption is **379µW**.

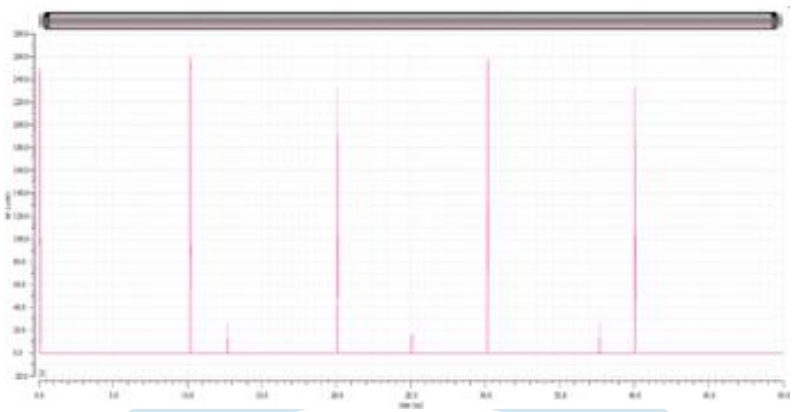


Fig 15: 2-bit binary multiplier power consumption

$$P_0=A_0+B_0$$
$$P_1=Sum(A_0B_1+A_1B_0)$$
$$P_2=Sum(A_1B_1+C_1)$$
$$P_3=C_3$$

The Fig 15, represents the power consumption of the 2-bit binary multiplier. The total power consumption is **1.1µW**.

The analysis of the designed basic cells for SIMD MAC unit provides required speed for high throughput of the system and maintains a decent power budget. The overall delay computed from the critical path is about **1ns** which is less than **3.6ns** in [1]. Hence, full custom design with much smaller nodes can provide improved performance with better power performance as well.

I. RESULTS

The analysis of the designed basic cells for SIMD MAC unit provides required speed for high throughput of the system and maintains a decent power budget. The overall delay computed from the critical path is about 1ns which is less than 3.6ns. Hence, full custom design with much smaller nodes can provide improved performance with better power performance as well.

Table 1: Comparison of Power & Delay

INSTANCE	DELAY(ps)	POWER(nW)
Inverter	Tr = 13.04 Tf = 13.12	16.2
AND gate	27.76	84.42
XOR gate	30.14	77
TG Adder	Tsum = 56.73 Tcarry = 51.05	207.4
CPL Adder	Tsum = 78 Tcarry = 57	0.474
Ripple Carry Adder 8-bit	Tsum = 337.6 Tcarry = 323.4	0.379
2-bit binary multiplier	68.05	0.11

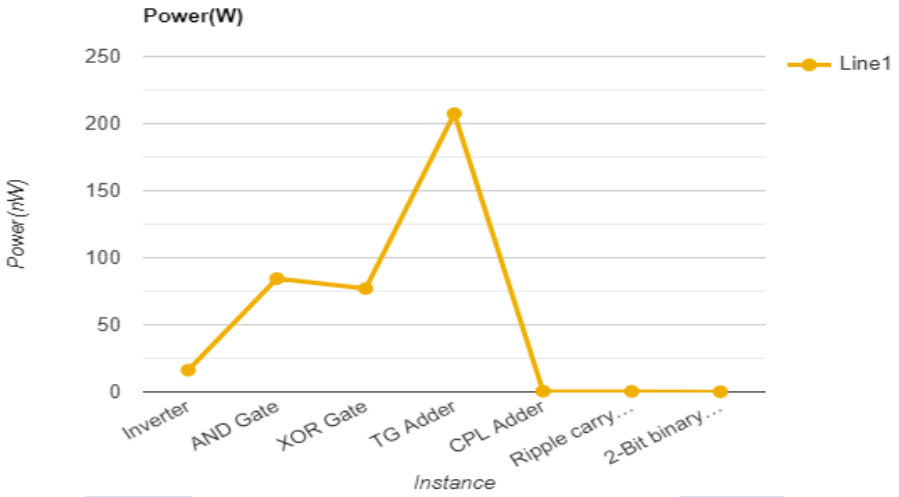


Fig 16: Graph between Power vs Instance

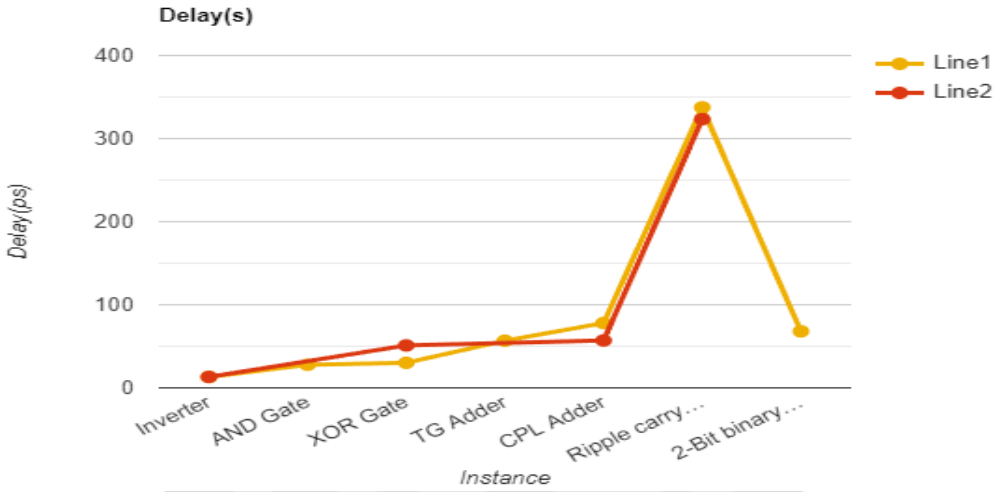


Fig 17: Graph between Delay vs Instance

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