A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filters

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***Abstract*—In this paper, asymmetric hybrid form for high Performance finite impulse response(FIR) filter switch symmetric Coefficients is proposed, which can be utilized in both fixed and Reconfigurable FIR implementations to solve the driving capacity Problem caused by the high fan out signals in the existing Symmetric transposed form based FIR architecture. The Evaluation results show that, when compared with the existing High speed FIR designs such as the symmetric systolic form in[13] And the hybrid for min[1], the proposed form can achieve Significant area and power savings with great ADP and PDP reduction. Moreover, when compared with the symmetric systolic For min[13] the required latency can be approximately reduced by33.3%,whichclearlyshowstheperformanceimprovementof The proposed method.**

Keywords — FIR filter , symmetric hybrid FIR.

I. INTRODUCTION

Finite Impulse Response (FIR) filter has been widely applied in digital signal processing systems due to its linear phase and stability characteristics. The FIR structure is very regular and can be viewed as the connection of several identical units for the basic tap operation. As shown inFig.1(a)and(b),a FIR filter can be implemented in a direct form or in a transposed form, in which the corresponding basic-unit in each form is also shown and indicated in the dotted box. Obviously, the critical data path in the direct form increases with the tap number (L), which consistsofonemultiplierand$1+\lfloor\log_2 L\rfloor$ adders. It will lead to a very long delay, when *L* becomes large. However, no matter how large *L* is, the critical data path in the transposed form always contains of one multiplier and one adder. Therefore, the transpose form can achieve higher performance than the direct form, which is also one of the reasons that most FIR filter architectures such as [2]-[8] are based on the transposed form.

In general, the tap number L is assumed to be large so as to meet the accuracy requirement in the frequency domain. For example, a 512-tap digital filter was presented in [9]. For the transposed form, however, the input register needs to drive all the following multipliers. Therefore, when L becomes large, the driving capacity problem due to the high fan outs would lead to a very long delay and then cause the performance degradation. To solve this problem, the systolic form [1], [10] and the hybrid form [1], [11] have been proposed as shown in Fig. 1 (c) and (d), where the corresponding basic-unit of each form is indicated in black dotted box. As the advantage of systolic form, no matter how large *L* is, the input only drives one multiplier

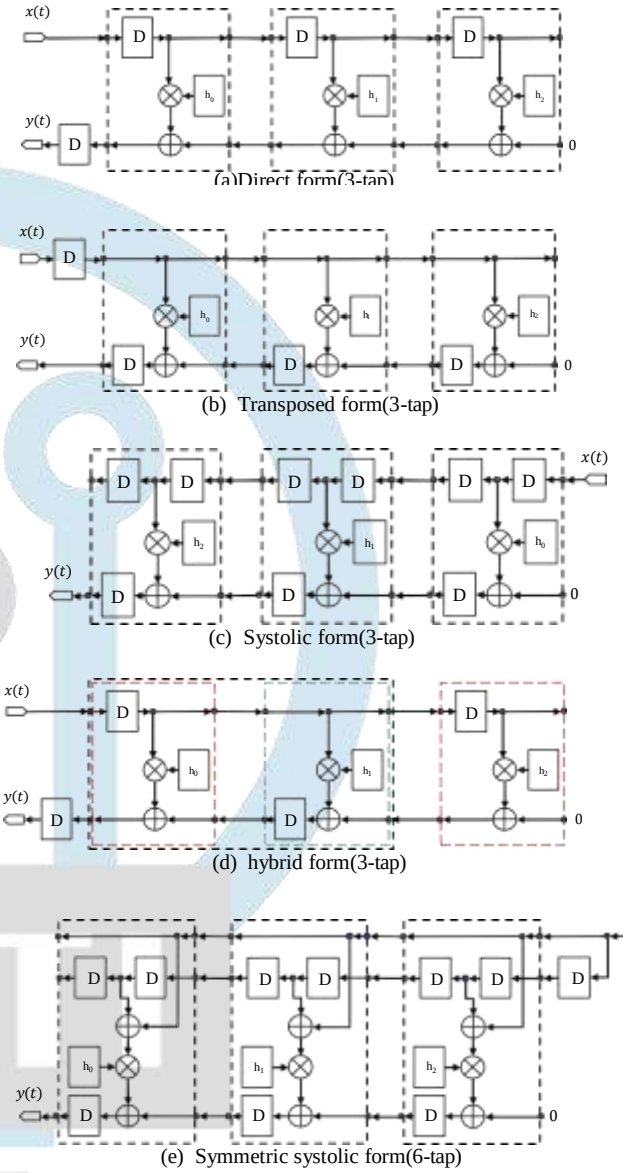


Fig.1. Various FIR implementations:(a)direct form,(b)transposed form,(c)systolic form, (d) hybrid form and (e) symmetric systolic form.

and one register. Moreover, the critical path contains only one multiplier and one adder. However, the corresponding hardware cost increases as two additional registers (i.e. one in

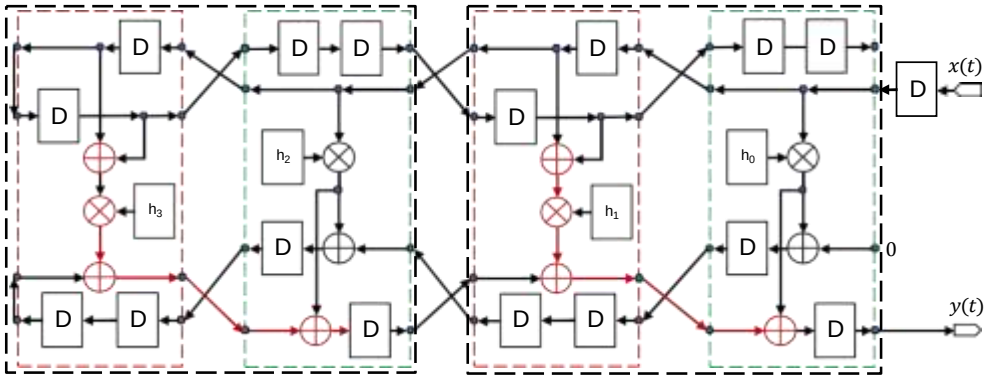


Fig.2.The proposed symmetric hybrid form (SHF) of an8-tapFIR filter.

the input side and the other in the adder tree) are required in each tap unit, which leads to larger area overhead and higher power consumption and introduces longer latency as well. On the other hand, the hybrid form can be viewed as the combination of the transposed form with the direct form, which can be obtained by changing the position of a small number of registers to the input side of a multiplier or to the output of an adder in tap units. Compared with the systolic form, the hybrid form made an optimal tradeoff between the performance and the area overhead. As a result, less registers are required, which makes the hybrid form more suitable for area-performance efficient implementations.

For a linear-phase FIR filter, the impulse response can be symmetric, which can be exploited for multiplier reduction. And the implementations of symmetric systolic form as shown in Fig. 1 (e) have been proposed in [12] and [13]. However, either the driving ability problem or the large area overhead problem still exists. The symmetry of coefficients, which can lead to a significant saving in hardware cost, has not been taken into consideration in the existing hybrid form FIR designs yet. Therefore, we explore the possibility of realization of a symmetric hybrid FIR filter in order to take advantage of the
symmetric coefficients for area-performance efficient FIR implementation in this paper.

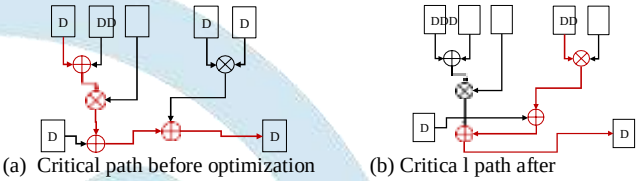
This paper is organized as follows: Section II describes the proposed area-performance efficient symmetric hybrid form realization of arbitrary FIR Filters. Evaluation results are presented in Section III. Finally, Section IV concludes the paper.

II. Proposed Symmetric Hybrid FIR

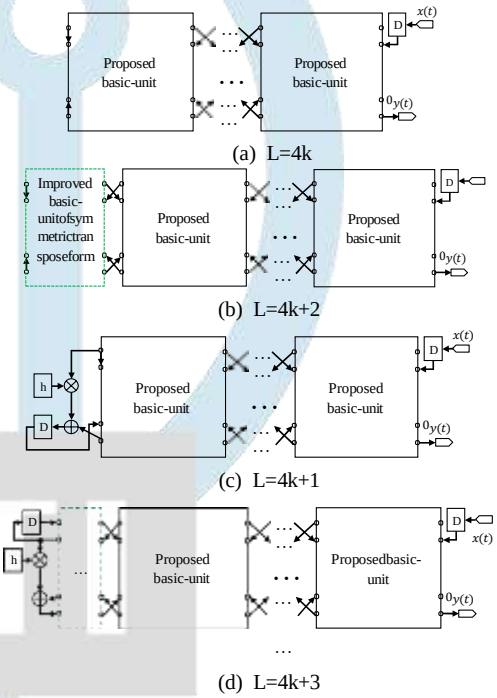
The number of registers in a *L*-tap hybrid form FIR is *L+1*, which is one third of that in the systolic form, and the corresponding latency is only *L* clock-cycle. Therefore, the proposed design extends the hybrid form for symmetric realization, by first solving the connection and timing matching problem between tap units; second, improving the performance through addition order changing; and third, extending for FIRs with arbitrary taps.

A. Proposed symmetric hybrid form

The basic-unit of hybrid form (HF) as shown in Fig. 1 (d) is the combination of the direct form(DF) and the transposed



(a) Critical path before optimization (b) Critica l path after optimization Fig. 3. Optimization of critical data path.



(a) L=4k

(b) L=4k+2

(c) L=4k+1

(d) L=4k+3

Fig.4. Arbitrary-tap FIR implementations in the proposed SHF.

from (TF). Therefore, it seems possible to implement the symmetric hybrid form (SHF) in a similar way by combining the symmetric direct form (SDF) [1] and the symmetric transposed form(STF)[1],[2],[8].It, however, should be noted that, unlike the direct form, the tap units in the symmetric form can't be directly connected, otherwise timing confusion will occur. In SDF, the basic-unit of symmetric direct form has two path sin input form and only one path in output form. However, the basic unit of symmetric transpose form have two paths in output form and only one path in input form.

The implementationofan8-tap symmetric hybrid form FIR filterisshowninFig.2asanexampleoftheproposedarea-

TABLE I
THE COMPARISONS OF HARDWARE COMPLEXITY(L-TAP)

FIR Form	Register Number	Adder Number	Multiplier Number	Latency (clock-cycle)	Driver Resources	Critical DataPath
SF[1]	$3L-1$	$L-1$	L	$2L$	$1mul+1reg$	$1mul+1add$
SSF[12]	$3\rceil L/2\rceil+1$	$L-1$	$\rceil L/2\rceil$	$L+1$	$\rceil L/2\rceil add+1reg$	$1mul+2add$
SSF[13]	$3L-2$	$L-1$	$\rceil L/2\rceil$	$L+\rceil L/2\rceil$	$1add+1reg$	$1mul+2add$
HF[1]	$L+1$	$L-1$	L	$L+1$	$2mul+1reg$	$1mul+2add$
Proposed SHF	$2L-1$	$L-1$	$\rceil L/2\rceil$	$L+1$	$1mul+1add+1reg$	$1mul+2add$

* Note that the required bit width of adders varies with methods
*Register Number : include input and output registers
* Latency: the clockcyclesbetweenthefirstvalidinputsampleandthefirstvalidoutputsample,assuming contiguous inputsamples.

performance efficient SHF design, which can be viewed as a combination of the symmetric direct form and the symmetric transposed from. In the proposed design, the basic unit (the black dotted box in Fig. 2) can perform 4-tap operations, in which the red and the green dotted boxes are like that in SDF and STF, respectively.

In the proposed SHF, two extra paths are formed: one is on the input side of the basic-unit in symmetric transpose form; and the other one is on the output side of the basic-unit in symmetric direct form. Because the basic-unit in either SDF or STF can conduct 2-tap processing, two extra registers in each incremented path have been inserted to match the timing of neighboring basic-units. Therefore, the proposed basic-unit of SHF contains of two multipliers, four adders and eight registers for 4-tap computation.

As shown in Fig.2, the critical data path in the proposed SHF FIR design contains of one multiplier and three adders. To further shorten the critical path for performance improvement, the corresponding addition order can be changed as that shown in Fig.3. Fig.3 (a) and (b) show the corresponding critical path before and after the addition order adjustment, respectively. It can be observed from the figure that, through the addition order adjustment, the critical data path in the proposed SHF can be reduced to only one multiplier and two adders.

It should be mentioned that the shortened critical path is obtained at the cost of adders' area because the bit-width of adders before and after multipliers are different, where adders placed before multipliers are in B-bit, while adders placed after multipliers should be in 2*B*-bit. Therefore, in a more precise way, the critical path in the proposed SHF design consists of one multiplier and two adders after multipliers, which is the same as that in hybrid form; but is longer than that in symmetric systolic form due to the bit-width difference in adders.

B. Extended SHF for arbitrary-tap FIR implementations

The basic unit in the proposed SHF design support 4-tap operations. Therefore, it seems that the proposed symmetric hybrid form can only be applied to FIRs with multiple of 4 taps. In order to solve this problem, extended forms of the proposed SHF for arbitrary-tap FIRs are presented in Fig. 4. AsshowninFig.4 (a),when L=4,8,12,…the FIR filter can be directly constructed by using the proposed SHF basic-unit. In Fig. 4 (b), when L=2,6,10,… except the proposed SHF basic-unit,anextracircuitisnecessaryfortheleft2-tapcalculation.

TABLEII
IMPLEMENTATIONRESULTSOF16-&512-TAPFIRFILTERS

L (Tap)	FIR Form	Delay (ns)	Area (um^2)	Power (mw)
16-tap	SF[1]	6.9	352529	19.6
	SSF[13]	7.8	240810	18.2
	HF[1]	8.6	236924	13.8
	SHF	8.8	169850	11.8
512-tap	SF[1]	6.9	11224875	359.1
	SSF[13]	7.8	6915051	255.8
	HF[1]	8.8	7606045	208.8
	SHF	8.9	5472521	184.4

The basic-unit of symmetric transpose form can be used here. Because the final basic-unit in the proposed SHF design is in the symmetric direct form, connecting it by the same type basic- unit will cause the critical data path increases by one adder. The design as shown in Fig. 4 (c) depends on the situation when L=1,5,9,…, in which the proposed SHF design is connected with one tap unit in the transposed form. When L=3,7,11,…one tap unit in the direct form can be adopted.

Therefore, regardless of the tap number of desired FIR filters, the critical data path of the proposed symmetric hybrid form FIR filter always contains of one multiplier and three adders. Moreover, the registers in the proposed SHF are only need to drive one adder, one multiplier, and one register, which successfully solves the driving capacity problem in large FIRs.

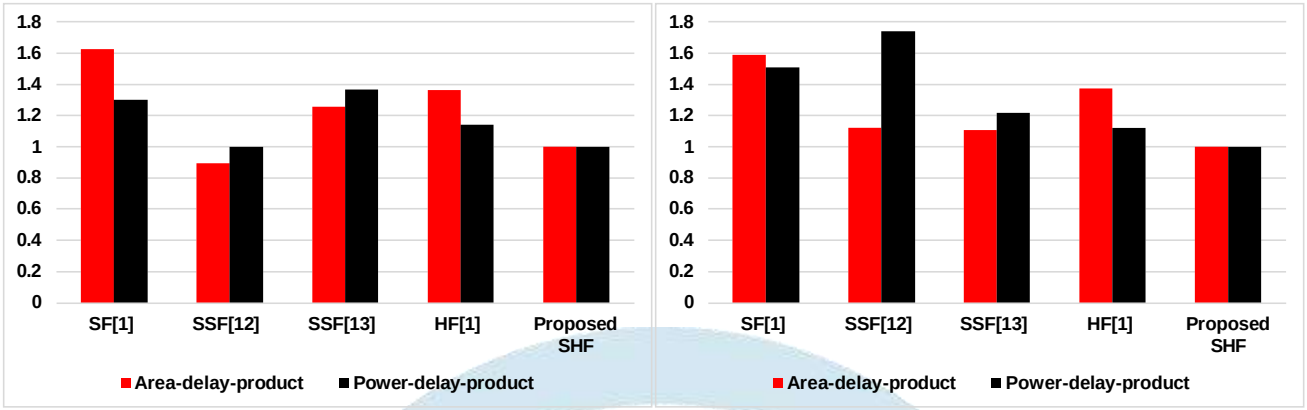
III. EVALUATION AND COMPARISON RESULTS

To examine the effectiveness of the proposed symmetric hybrid form FIR filter, various implementation results and comparisons are provided in this section.

A. Comparison of hardware complexity

The overall hardware complexity of the proposed SHF is compared with systolic form (SF)[1], symmetric systolic form (SSF) [12], [13], and hybrid form (HF) [1] in Table. I.

When compared with the canonic structure, the proposed SHF design needs additional L registers to achieve the purpose of half-subtracting multipliers; while it can save L registers when compared to the symmetric systolic form[13]. Except for the symmetric systolic form[12],which has the driving ability problem, the proposed SHF design is the most economical in terms of hardware resources. Moreover, the latency of the proposedSHFdesignisonlyL+1clock-cycle.Asthetrade-off,



(a)16-tap implementation (b)512-tap implementation

Fig. 5. Normalized area-delay and power-delay product of the five implementation methods for 16- & 512-tap FIRs.

The critical data path consists of one larger size adder compared with hybrid form [1] and symmetric systolic form [13].

B. Implementationresultsof16-&512-tapFIRs

For evaluation and comparison purposes, 12-bit (input, output and coefficients) reconfigurable FIR filter sin16and512 taps are implemented by applying the proposed symmetric hybrid form and the existing forms, and the corresponding logic synthesis results such as area, critical path delay and power consumption are shown in Table II for comparisons. For a more comprehensive evaluation, area-delay product (ADP), and power-delay product (PDP) have been compared in Fig. 5.

AsshowninFig.5,because16-tapisnotverylarge,andthe symmetric systolic form [12] has minimal hardware resources in this five FIR filter forms, it has the best performance no matter in ADP and PDP. However, when applied to 512-tap designs, due to the driving capacity problem, compare to other FIR designs, the delay of SSF [12] became extremely long. Therefore, the PDP are the worst of all the five designs.

When compared with symmetric form[13],it is obvious that the proposed SHF design can improve the performance and shorten the latency while the required register number can also bereducedgreatly.Thus,forthe16-tapFIR,theproposedSHF canachieve29%areareductionand35%powersavingwiththe corresponding 20% ADP and 27% PDP improvements. The proposed SHF can also reduce the latency by 7 clock cycles. When the tap number increases to512, the corresponding saving in area, power, ADP and PDP becomes to21%, 28%, 10% and 18%, and the latency can be shortened by 255 clock cycles. When compared with the hybrid form[1], the proposed design can reduce the number of multipliers by half, therefore the corresponding saving in area, power, ADP and PDP is 28%, 12%, 27% and 11%, respectively, which clearly shows the effectiveness of the proposed SHF design.

IV. Conclusion

This paper proposed a symmetric hybrid form for high speed FIR filters by solving the driving capacity problem in large tap symmetric FIR filter designs. Comparing with the existing SSF and HF, the proposed SHF form can achieve great area reduction and power saving with ADP and PDP improvements. Moreover, when compared with SSF the required latency can be Approximately reduced by33.3%, which clearly shows the performance improvement of the proposed method.

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