Channel Thickness Engineering for Enhanced Digital Performance in Double-Gate Tunnel Field Effect Transistor

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***Abstract*—This work proposed a Double Gate Tunnel Field effect Transistor (DG-TFET) for which the simulations showed significant improvements in threshold voltage, subthreshold swing, ON current (I_{ON}) and OFF current (I_{OFF}) compared to conventional MOSFETs. Unlike conventional MOSFETs that rely on thermionic emission, DG-TFETs utilize band-to-band tunneling (BTBT) as the carrier transport mechanism, enabling subthreshold swings below 60 mV/decade and significant reductions in power consumption. Using the Silvaco Atlas 2D simulator, it has been observed that due to scaling of channel thickness from 16 nm down to 8 nm, though there is a compromise in the ON- current, OFF- current for 8 nm thick device improves by 89.59 % compared to 16 nm thick device for V_{DS} = 0.5 V and V_{GS} = 0 V. However, the more thickened device outperforms the less thickened one in terms of I_{ON}-I_{OFF} ratio and intrinsic delay.**

***IndexTerms*—Double-Gate TFET, Band-to-Band Tunneling (BTBT), Channel Thickness Engineering, barrier lowering.**

I. INTRODUCTION

The continuous downscaling of conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has approached fundamental physical and thermodynamic limits, particularly concerning subthreshold swing (SS) and leakage current control [1],[2],[3]. As device dimensions enter the nanoscale regime, short-channel effects, drain-induced barrier lowering (DIBL), and increased static power consumption severely degrade the performance and energy efficiency of modern integrated circuits. The thermionic emission mechanism governing carrier transport in MOSFETs constrains the subthreshold slope to a minimum of 60 mV/decade at room temperature, making it difficult to achieve ultra-low-power operation. This has driven extensive research into alternative device architectures capable of breaking the 60 mV/decade barrier while maintaining compatibility with complementary metal–oxide–semiconductor (CMOS) technology [4].Tunnel Field-Effect Transistor (TFET) is essentially a gated P-I-N diode that takes advantage of a band-to-band tunneling (BTBT) mechanism as the main carrier transport method to overcome the sub-threshold swing limitation of a conventional MOSFET.

Among various TFET architectures, the Double-Gate TFET (DG-TFET) configuration provides enhanced electrostatic control over the channel and improved tunneling efficiency due to the dual-gate coupling effect [5],[6],[7]. In this configuration, two symmetrically placed gates modulate the potential barrier across a thin intrinsic region, creating a more uniform electric field distribution and facilitating efficient tunneling between source and drain [8],[9],[10]. The symmetric gate structure reduces leakage, short-channel effects, and improves the ON-current compared to single-gate devices [11], [12]. Recent studies have shown that the analog performance[13] of DG-TFETs—characterized by parameters such as subthreshold swing, transconductance (gm), transconductance generation factor (TGF), and ON/OFF current ratio (I_{ON}/I_{OFF})—is highly sensitive to the structural and material parameters of the device, including channel thickness (t_{ch}) and gate dielectrics [14],[15],[16].

In this paper, a detailed analysis of digital parameters of Double-Gate Tunnel Field-Effect Transistors (DG-TFETs) with varying channel thicknesses using the Silvaco Atlas 2D simulator is presented. The channel thickness (t_{ch}) is varied parametrically across 8 nm, 12 nm, and 16 nm to evaluate its effect on digital performance characteristics parameters such as ON-OFF ratio and intrinsic delay. The objective is to identify the optimal thickness configuration that improves threshold voltage and intrinsic delay and I_{ON}-I_{OFF} ratio while maintaining favorable leakage and switching characteristics. The outcomes of this study provide valuable design insights for future high-gain, energy-efficient DG-TFETs, as better alternative to CMOS technology in next-generation digital applications.

II. DEVICE STRUCTURE AND SIMULATION

The proposed Double-Gate Tunnel Field-Effect Transistor (DG-TFET) structure investigated in this work is a planar, symmetric, p–i–n configured device designed and the electrical performance of DG-TFET was simulated using Silvaco TCAD Atlas 2D software. The device schematic, shown in **Fig. 1**, depicts the structural configuration of the DG-TFET, including the source, channel, drain, and gate regions. The DG-TFET, adopted in this simulation comprises three primary regions: a heavily doped p^+ source, a lightly doped intrinsic channel, and a heavily doped n^+ drain, forming a reverse-biased p–i–n junction that facilitates band-to-band tunneling(BTBT) when an appropriate gate bias is applied. The quantum mechanical transistor (QMT) has reached such small dimensions for doping concentration gradients are: $7.5\times10^{20} cm^{-3}$, $10^{10} cm^{-3}$ and 5 x $10^{18} cm^{-3}$ for the source, intrinsic, and drain regions respectively. Doping has been optimized to create the maximum ON-current (I_{ON}) , while keeping OFF current $(I_{OFF}$) low.In order to have a minimal I_{OFF}, the doping of the source is slightly lower compared to that of the drain. The intrinsic region acts as the active tunneling channel controlled electrostatically by two identical gates positioned on the top and bottom surfaces of the channel.The double-gate configuration provides enhanced electrostatic control over the channel potential, thereby reducing short-channel effects and improving the tunneling efficiency compared to single-gate TFETs. Both gates are isolated from the channel by a thin high-κ dielectric layer (HfO_2) of thickness 2 nm, instead of using conventional SiO_2which ensures strong gate-to-channel coupling while minimizing gate leakage.

In the simulation, band-to-band tunneling and trap-assisted tunneling models are used to calculate tunneling current from the source to drain. To capture the effects of concentration and temperature in mobility, Caughey-Thomas model and parallel electric field model are used for low and high electric fields, respectively. For carrier transport, drift-diffusion model with quantum correction has been used.

The key design parameters used in the simulations are summarized in **Table 1**.

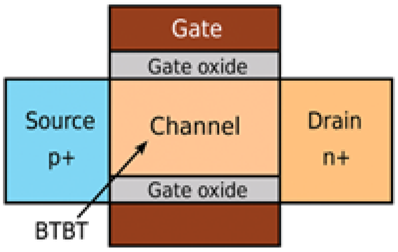

Figure 1 Schematic Diagram of the DG TFET

Table 1 Design parameters considered for simulation

Parameters	***Values***
Gate length ($\boldsymbol{L_G}$)	50 nm
Drain and source lengths ($\boldsymbol{L_D}$, $\boldsymbol{L_S}$)	100 nm
Oxide thickness ($\boldsymbol{t_{ox}}$)	2 nm
Channel thickness ($\boldsymbol{t_{ch}}$)	8 nm, 12 nm, and 16 nm
Source concentration ($\boldsymbol{N_S}$)	7.5 x $10^{20} cm^{-3}$
Intrinsic concentration ($\boldsymbol{n_i}$)	$10^{10} cm^{-3}$
Drain concentration ($\boldsymbol{N_d}$)	5 x $10^{18} cm^{-3}$
Gate voltage ($\boldsymbol{V_G}$)	1.0 V
Supply voltage ($\boldsymbol{V_{dd}}$)	0.5 V
Oxide gate	HfO_2
Work function of the Metal	5.2eV
Silicon Thickness (t_{Si})	10 nm

III. RESULTS AND DISCUSSIONS

The variation of drain current with varied channel thicknesses in the range of 8 nm to 16 nm at V_{DS} =0.5 V is shown in **Fig. 2**. It is evident that as channel thickness is scaled down from 16 nm to 8 nm, the bandgap of the devices gets increased due to effect of scaling. Also, threshold voltage of the devices measured at constant current of 1e-7 A/µm at V_{DS} =0.05 V increases from 0.17 V to 0.26 V as the channel thickness gets changed from 16 nm to 8 nm. Due to increase of bandgap and thus threshold voltage with decrease of channel thickness, drain current of the devices also gets decreased, as shown in Fig. 2. So, ON- current measured at V_{DS} = V_{GS} = 0.5 V is 5.96 times lower in 8 nm thick device compared to 16 nm one. However, with reduction of channel thickness, the effect of electric field on the channel increases showing better control over short channel effects. From **Fig. 3**, it can be shown that the peak electric field changes from 2.30×10^6 V/cm to 1.78×10^6 V/cm as channel thickness changes from 8 nm to 16 nm. As electric field has better control in less thickened device, so barrier lowering is less in such a device as shown in **Fig. 4**. Barrier lowering across the channel for 8 nm device is 1.07 times less compared to the more thickened one. Less barrier lowering signifies lesser short channel effects in narrowed channel device. So, OFF-current measured at V_{DS} = 0.5 V and V_{GS} = 0 V is 9.6 times less in 8 nm device compared to 16 nm. I_{ON}-I_{OFF} ratios for the devices are shown in **Fig.5**. It can be concluded that though less thickened device shows better OFF state characteristics, the more thickened one outperforms it in terms of this ratio. I_{ON}-I_{OFF} ratio for 16 nm thick device is thus 6.23 times more compared to 8 nm one indicating that the thickened device has better ability to switch between ON and OFF states. Thus, intrinsic delay of the devices, shown in **Fig. 6**, shows that 16 nm device has intrinsic delay to be 5.96 times less compared to 8 nm device making the thicker device more efficient for digital circuit operation.

All computed parameters are summarized in **Table 2**.

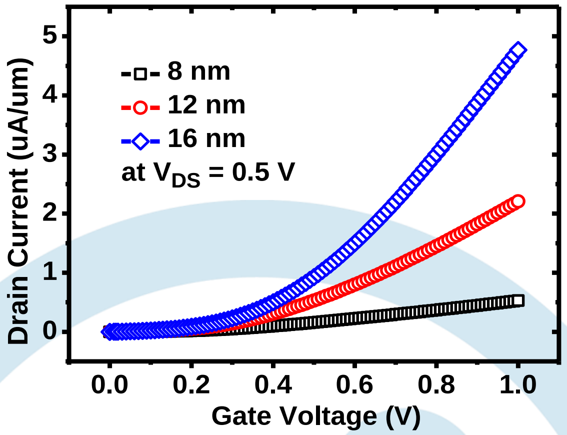

Figure 2 Transfer characteristics of Double-Gate Tunnel Field-Effect Transistor (DG-TFET) with channel thickness varying as 8 nm, 12 nm and 16 nm and gate length as 50 nm for V_{DS} = 0.5 V.

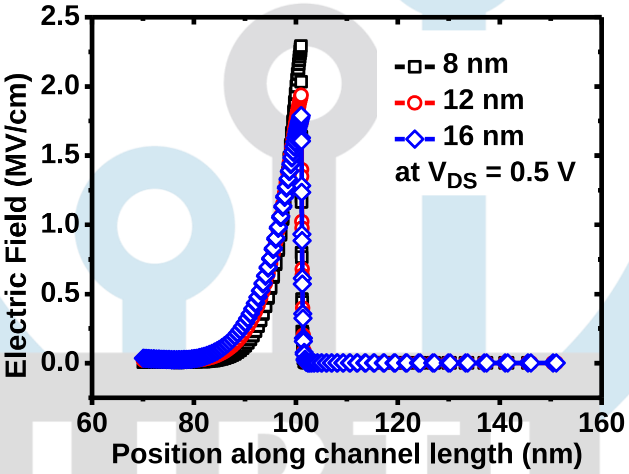

Figure 3 Electric Field profile of Double-Gate Tunnel Field-Effect Transistor (DG-TFET) with channel thickness varying as 8 nm, 12 nm and 16 nm and gate length as 50 nm for V_{DS} = 0.5 V.

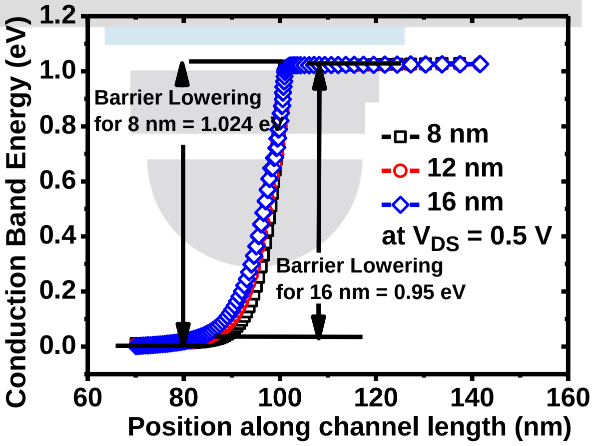

Figure 4 Barrier Lowering of Double-Gate Tunnel Field-Effect Transistor (DG-TFET) with channel thickness varying as 8 nm, 12 nm and 16 nm and gate length as 50 nm for V_{DS} = 0.5 V.

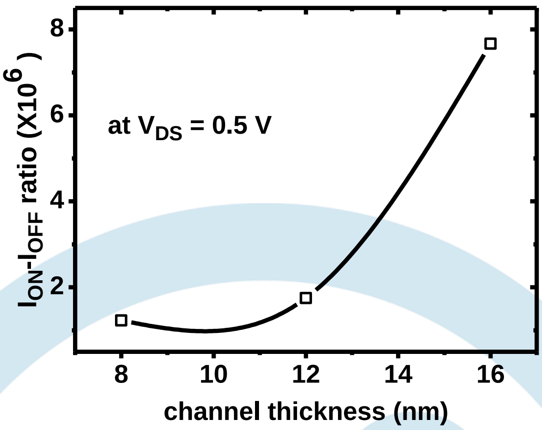

Figure 5 I_{ON}-I_{OFF} ratio of Double-Gate Tunnel Field-Effect Transistor (DG-TFET) with channel thickness varying as 8 nm, 12 nm and 16 nm and gate length as 50 nm for V_{DS} = 0.5 V.

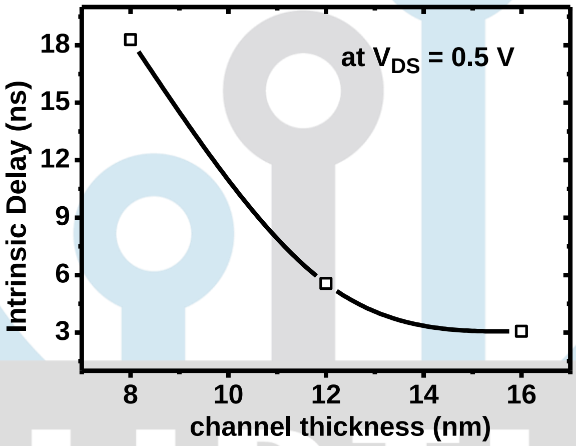

Figure 6 Intrinsic Delay of Double-Gate Tunnel Field-Effect Transistor (DG-TFET) with channel thickness varying as 8 nm, 12 nm and 16 nm and gate length as 50 nm for V_{DS} = 0.5 V.

Table 2 Computed parameters of the DG-TFET

Parameter	***Unit***	***8nm***	***12 nm***	***16nm***
Threshold Voltage (V_{th})	V	0.17	0.24	0.26
ON-Current (I_{ON})	A/µm	1.57×10^{-7}	5.16×10^{-7}	9.36×10^{-6}
OFF-Current (I_{OFF})	A/µm	1.27×10^{-13}	4.39×10^{-13}	1.22×10^{-12}
ON/OFF Ratio (I_{ON}/I_{OFF})		1.23×10^{6}	1.75×10^{6}	7.67×10^{6}
Intrinsic Delay	ns	18.29	5.56	3.06

IV. CONCLUSION

We have simulated Double-Gate Tunnel Field-Effect Transistors (DG-TFET) with varied channel thicknesses viz. 8 nm, 12 nm and 16 nm at gate length of 50 nm. The findings show that device with 8 nm channel thickness demonstrates better OFF state characteristics with compromise in ON-state characteristics. However, 16 nm thick device shows better ON-OFF ratio and lowered intrinsic delay and better ON-current with a compromise in OFF-state characteristics. So, to make DG-TFETs a better alternative to CMOS technology for next-generation digital as well as analog applications, we would like to propose 12 nm thick DG-TFET as the alternate device as it shows a considerable ON-current of 5.16×10^{-7} A/µm, relatively high ON-OFF ratio of 1.75×10^{6}, comparatively low intrinsic delay of 5.56 ns and also reduced OFF-current of about 4.39×10^{-13} A/µm.

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