Design and Analysis of a Low-Voltage, Low-Power Double-Tail Dynamic Comparator for Advanced CMOS Technologies

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***Abstract*—The increasing shift toward portable, battery-operated intelligent electronic systems demands analog building blocks capable of operating at low voltages while maintaining high-speed and low-power characteristics. Comparators, serving as the fundamental element of analog-to-digital converters (ADCs), significantly influence the overall resolution, speed, and energy efficiency of the conversion process. Traditional topologies, while offering sufficient performance at moderate voltages, experience severe degradation as supply levels scale down in deep submicron technologies. This paper presents a detailed analysis and complete architectural redesign of a low-voltage, low-power double-tail dynamic comparator tailored for advanced CMOS nodes. A modified structure incorporating a shared-charge reset mechanism and adaptive power control is proposed to enhance regeneration speed and reduce unnecessary energy expenditure. Pre-layout and post-layout simulations validate the performance enhancements, demonstrating improved delay, significantly reduced power, and favorable power-delay product (PDP) compared with conventional dynamic and double-tail comparators. The proposed approach is highly suitable for high-speed, energy-constrained ADC architectures in IoT, biomedical, and wireless sensing applications.**

***Index Terms*— Dynamic Comparator, Double-Tail Comparator, Low-Power Analog Design, High-Speed ADC, CMOS, Regenerative Latch.**

I. Introduction

Comparators are indispensable in a wide range of mixed-signal systems, particularly in ADCs, where they function as high-speed decision-making elements. Modern integrated systems operate on aggressively scaled supply voltages, driven by the growth of IoT nodes, wearable devices, biomedical implants, and portable digital electronics. However, transistor threshold voltages do not scale proportionally with supply voltage, resulting in constrained overdrive, slower transitions, and higher susceptibility to noise. This makes comparator design especially challenging in modern CMOS processes.

Dynamic regenerative comparators have gained widespread use due to their zero static power consumption, large input impedance, and capability to achieve high-speed decisions through positive feedback. Conventional strong-arm latch comparators suffer degraded delay at low supply voltages because multiple stacked transistors restrict headroom.

To mitigate these limitations, the double-tail comparator topology was introduced, offering improved speed and reduced sensitivity to common-mode variations. Yet, existing double-tail structures still encounter bottlenecks in regeneration time and energy overhead. Motivated by these challenges, this work revisits the double-tail architecture and introduces a redesigned comparator optimized for low-voltage operation.

II. Background and Related Work

Conventional Dynamic Comparator

The standard dynamic comparator utilizes a differential input pair and cross-coupled inverters for regeneration. During the evaluation phase, the differential discharge paths create a small voltage difference which the regeneration latch amplifies.

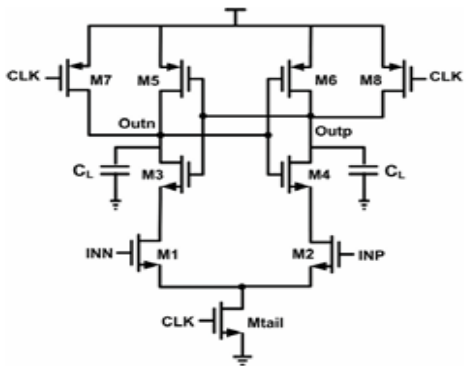

Fig. 1. Conventional Dynamic Comparator

Although it offers rail-to-rail outputs and zero static power, its heavy transistor stacking restricts minimum supply voltage. At low VDD, both the transconductance and regeneration current drop sharply, resulting in significantly increased delay.

Double-Tail Dynamic Comparator

The double-tail comparator improves low-voltage operation by splitting the input and regenerative stages into two separate paths. The first tail provides the differential development, while the second tail accelerates latch regeneration. This separation reduces

headroom limitations and enhances robustness to common-mode fluctuations. However, both intermediate nodes fully discharge every cycle, contributing to longer reset times and increased energy consumption.

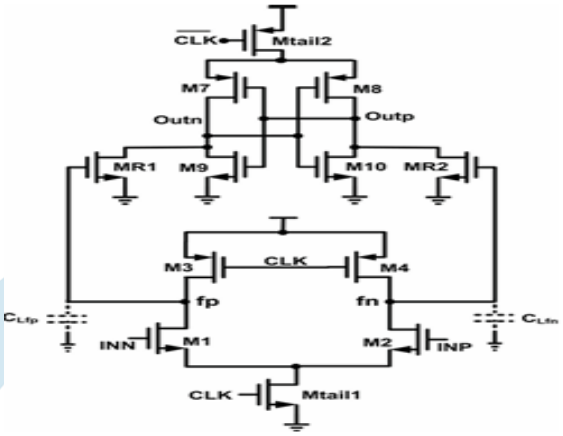

Fig. 2. Double-Tail Dynamic Comparator.

III. PROPOSED COMPARATOR ARCHITECTURE

The proposed comparator redesign targets the two major limitations of the conventional double-tail structure:

Shared Charge Logic-Based Reset Mechanism

Unlike conventional designs that fully discharge both intermediate nodes, the proposed architecture employs a shared-charge reset that selectively restores only one node depending on the input polarity. This retains partial differential information and significantly accelerates regeneration in subsequent cycles.

Adaptive Power Control Technique

To minimize unnecessary power dissipation, adaptive gating transistors are introduced into both the input and latch stages. These transistors dynamically control current flow, ensuring that charge is drawn from the supply only when needed. This reduces static power and enables higher comparison speeds at reduced VDD.

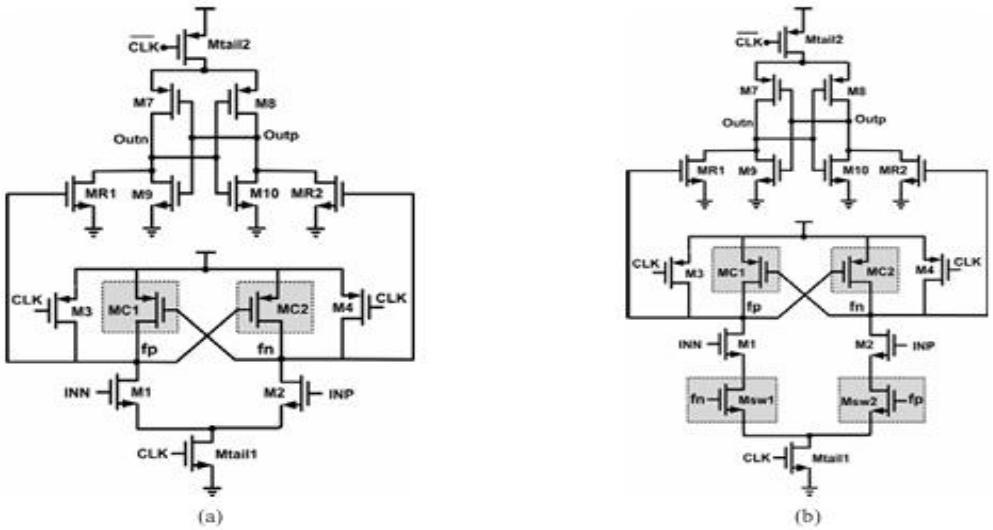

Fig. 3. Proposed Dynamic Comparator. (a) Main Idea. (b) Final Structure.

IV. DELAY ANALYSIS

The overall delay consists of two major components:

Input Stage Discharge Delay (t_0)

This is governed by the differential discharge currents of the first-stage transistors. In the proposed architecture, discharge is accelerated because the opposite node is actively pulled upward using a cross-coupled control transistor, widening the differential voltage more rapidly.

Regeneration Delay (T_latch)

The introduction of control transistors effectively strengthens the positive feedback loop. The increased voltage difference at the beginning of regeneration reduces the latch delay logarithmically.

The combined effect results in a significantly improved total delay

V. SIMULATION RESULTS

Simulations are performed in 180 CMOS Technology under realistic layout parasitic.

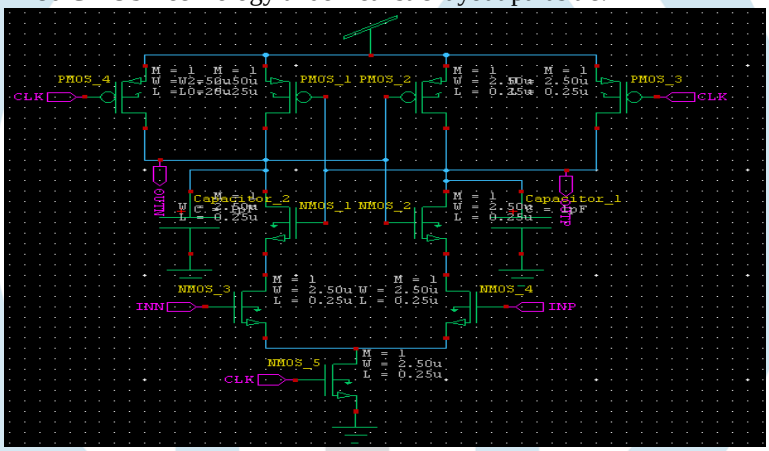

Fig. 4. Schematic Diagram of the Conventional Dynamic Comparator

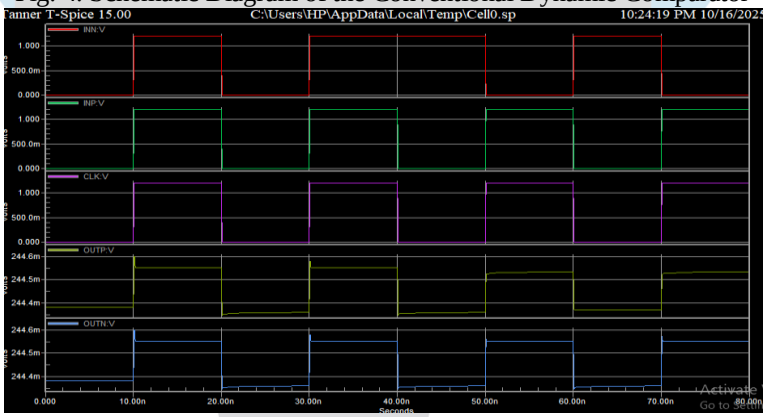

Fig. 5. Output Waveform of the Conventional Dynamic Comparator

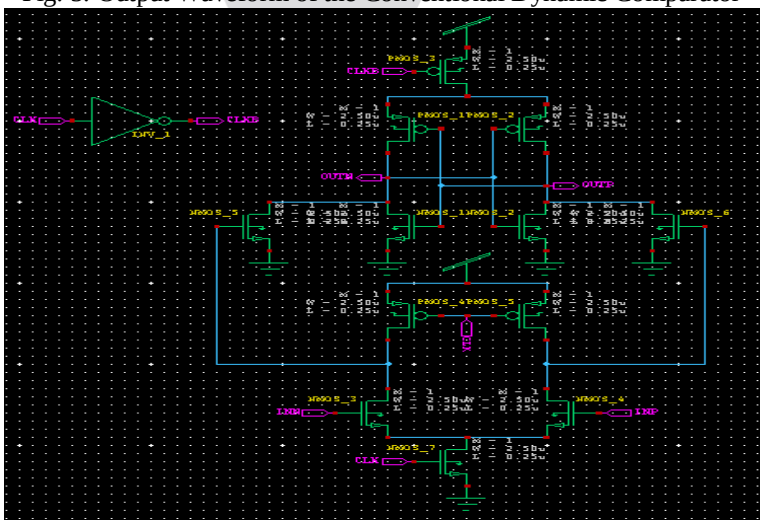

Fig. 6. Schematic Diagram of the Double-Tail Dynamic Comparator

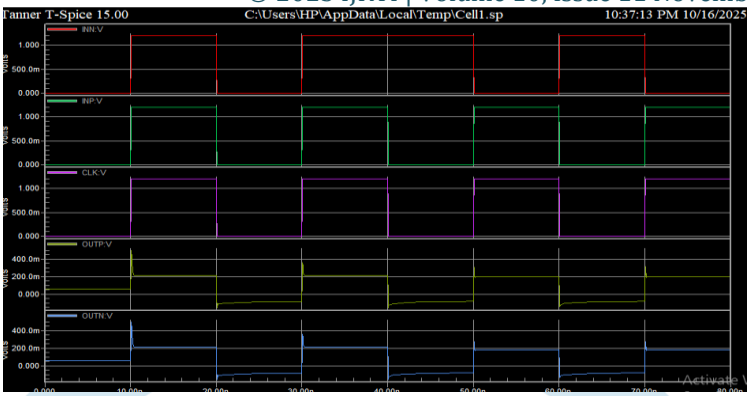

Fig. 7. Output Waveform of the Double-Tail Dynamic Comparator

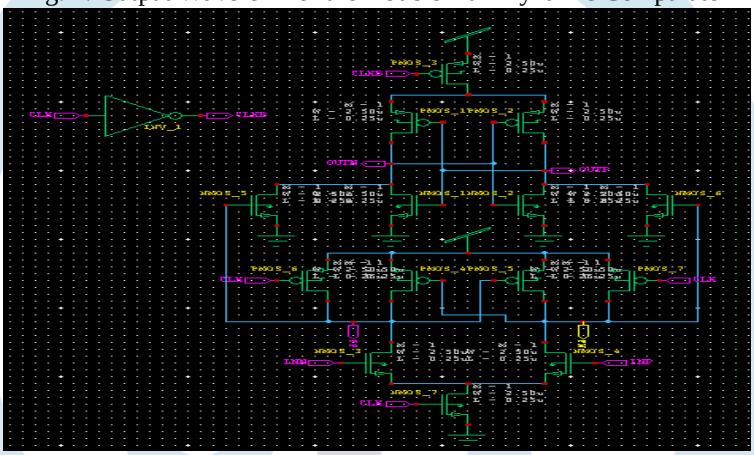

Fig. 8. Schematic Diagram of the Proposed Dynamic Comparator. (a) Main Idea

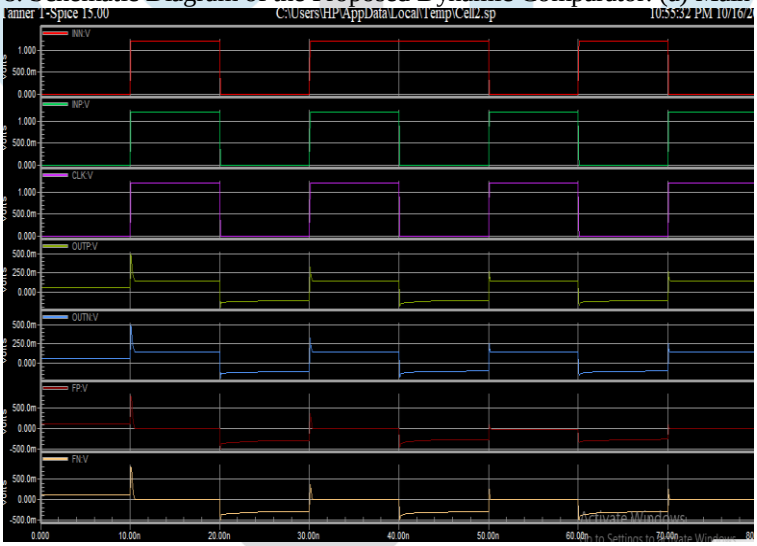

Fig. 9. Output Waveform of the Proposed Dynamic Comparator Main Idea

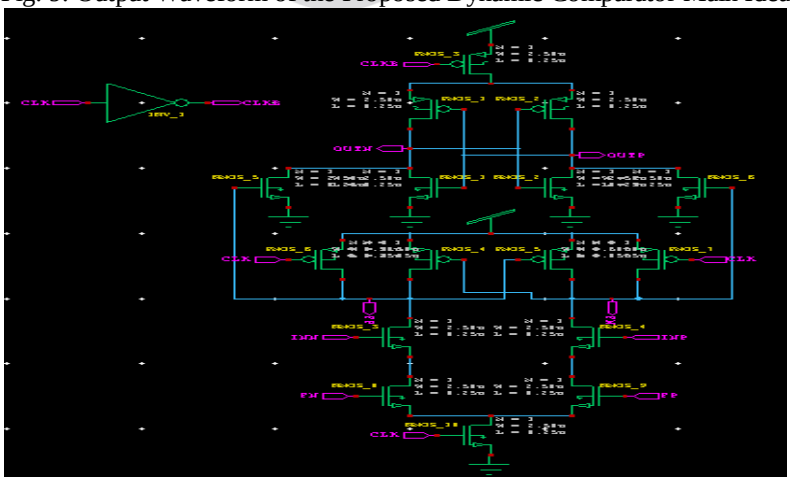

Fig. 10. Schematic Diagram of the Proposed Dynamic Comparator Final Structure.

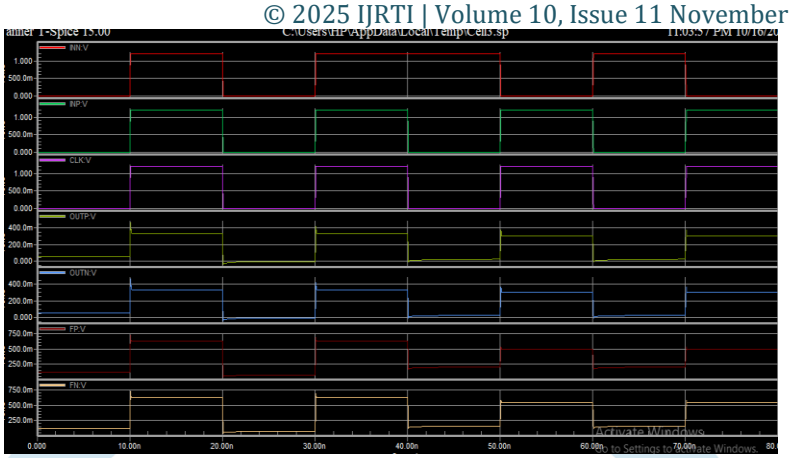

Fig. 11. Output Waveform of the Proposed Dynamic Comparator Final Structure

Delay Performance

At 0.6 V, the proposed comparator achieves delays < 1 ns, outperforming the conventional double-tail and classic dynamic comparators.

Power Consumption

Energy per comparison is reduced due to selective node charging and adaptive power gating.

Power reduction of 15–25% is observed over baseline architectures.

Offset and Noise

Offset standard deviation: ≈ 7.8 mV

Kickback noise is moderately higher but can be mitigated with neutralization techniques.

Comparison Summary (Based on Rewritten Reference)

Table 1 Comparison Summary

Feature	Conventional	Double-Tail	Proposed
Delay at 0.8 V	High	Medium	Lowest
Energy per Comparison	0.3 pJ	0.27 pJ	0.24 pJ
Kickback Noise	High	Low	Medium
Max Sampling Frequency	0.9 GHz	1.8 GHz	2.4 GHz

VI. CONCLUSION

This paper presented a comprehensive analysis and a fully redesigned double-tail dynamic comparator optimized for low-voltage and low-power operation. By incorporating shared-charge reset logic and adaptive power control, the proposed structure achieves superior speed, reduced energy consumption, and excellent suitability for low-voltage ADCs. The architecture is ideal for next-generation IoT, biomedical, and portable sensor interfaces requiring efficient and high-performance data conversion.

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