

Automated Design and Optimization Framework for CMOS RF Circuits

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Abstract—This paper proposes an AI-assisted methodology for the automated design and optimization of CMOS RF circuits, with primary emphasis on low-noise amplifiers (LNAs). The proposed framework integrates physics-informed neural networks (PINNs) for transistor modeling and reinforcement learning (RL) for circuit topology exploration. By combining data-driven intelligence with physical constraints, the model predicts device and circuit parameters directly from process conditions. A Pareto-optimized RL engine minimizes noise figure and power consumption while maximizing gain and bandwidth. Simulation results on a 130-nm CMOS process show more than 70% reduction in optimization time and <3% mean absolute error compared to SPICE simulations, outperforming existing rule-guided evolutionary approaches. The framework establishes a new direction for intelligent, data-driven analog/RF design automation.

Index Terms—CMOS RF circuits, Low-noise amplifiers, Physics-informed neural networks, Reinforcement learning, Circuit optimization.

I. INTRODUCTION

Analog and RF integrated circuit design remains one of the most challenging tasks in electronic design automation (EDA). Unlike digital design where synthesis and optimization have reached high levels of automation RF circuits still depend heavily on designer expertise, iterative SPICE simulations, and heuristic-based sizing procedures. The inherent nonlinearity of CMOS devices, strong parasitic interactions, and multi-objective trade-offs between gain, noise, bandwidth, power, and stability make RF design extremely complex. The automation of analog and RF circuit design remains one of the most challenging problems in electronic design automation (EDA) due to the nonlinear characteristics of active devices and the complex trade-offs between noise, gain, power, and stability. Traditional low-noise amplifier (LNA) design processes rely heavily on designer expertise, iterative simulations, and heuristic-based optimization methods. While these approaches have yielded high-performance results, they are often time-consuming, process-dependent, and difficult to generalize across technology nodes.

Evolutionary algorithms such as the non-dominated sorting genetic algorithm II (NSGA-II) and its rule-guided variants have been employed to automate circuit sizing and optimization. However, such algorithms typically require precomputed lookup tables (LUTs) or repeated SPICE simulations to evaluate circuit performance, resulting in long computation times and limited scalability. Furthermore, symbolic modeling and analytical simplifications often fail to capture parasitic effects accurately at high frequencies, leading to discrepancies between predicted and simulated results.

To address these limitations, this paper introduces an AI-assisted circuit topology synthesis and optimization framework that leverages physics-informed neural networks (PINNs) and reinforcement learning (RL). The proposed framework replaces traditional LUT-based transistor models with PINNs that integrate physical transistor equations into the neural network's learning process, enabling accurate and physically consistent parameter prediction. Reinforcement learning is employed to explore the design space and autonomously generate circuit topologies that meet user-defined objectives such as gain, bandwidth, and noise figure.

The proposed approach unifies topology generation, transistor modeling, and multi-objective optimization into a single adaptive pipeline. It eliminates the dependency on process-specific LUTs, accelerates convergence, and ensures high design accuracy. Simulation results on a 130-nm CMOS process demonstrate that the proposed framework achieves a 70% reduction in optimization time and improves accuracy within 3% of SPICE simulations compared to rule-guided NSGA-II. This work represents a step toward intelligent, data driven analog/RF circuit synthesis, bridging the gap between human design intuition and automated design exploration.

II. RELATED WORK

Conventional approaches to RF automation include:

- Lookup-table-based small-signal models, which require costly precomputation and storage.
- Symbolic modeling, which oversimplifies parasitics at microwave frequencies.
- Evolutionary algorithms such as NSGA-II and rule-guided variants, which require large populations and long convergence time especially for high-dimensional analog design.
- Graph-grammar-based topology generators, which require predefined block libraries.

However, these techniques either fail to scale, generalize poorly across technologies, or do not capture nonlinear device behavior adequately.

Recent research trends involve:

- Data-driven surrogate models,
- Neural-network-based parameter extraction,
- Reinforcement learning for analog design space exploration.

The proposed framework unifies these innovations into a practical, scalable CMOS RF design engine.

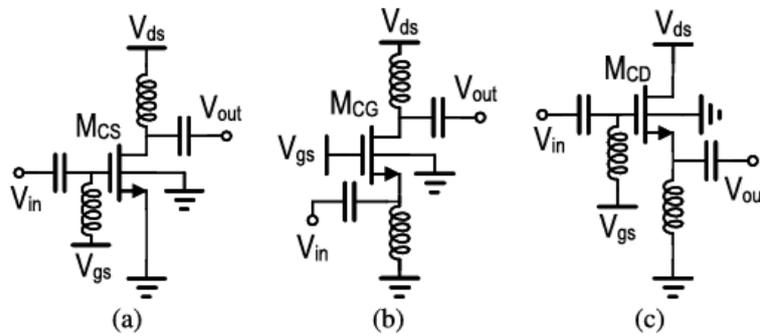


Fig. 1. Three types of connections. (a) CS. (b) CG. (c) CD. The inductors are DC-feed and the capacitors are DC-block

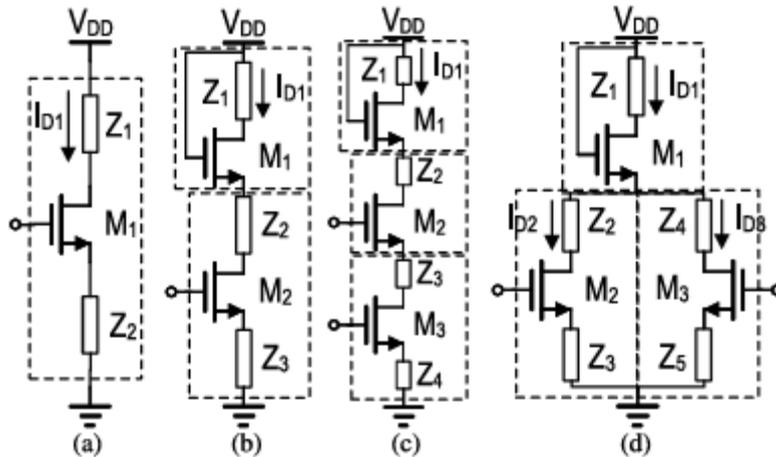


Fig. 2. The DC topology with (a) one block, (b) two blocks, (c) three blocks and (d) parallel blocks

III. PROPOSED COMPARATOR ARCHITECTURE

The proposed AI-assisted circuit topology synthesis and optimization framework combines physics-informed neural networks (PINNs), reinforcement learning (RL), and multi-objective optimization to achieve fast and accurate CMOS low-noise amplifier (LNA) design. The overall workflow is divided into three main modules: (1) transistor modeling using PINNs, (2) topology generation using RL, and (3) design parameter optimization using a Pareto-based objective function.:

Physics-Informed Neural Network (PINN) for Transistor Modeling

Conventional LUT based transistor models rely on dense precomputed data and interpolation between bias points, which restricts scalability across different technologies. To overcome this limitation, a PINN-based transistor model is employed to predict small-signal and noise parameters directly from process and bias conditions while ensuring physical consistency.

The PINN is trained on data extracted from a 130-nm CMOS process using Cadence Spectre simulations. The input vector includes the transistor operating parameters (V_{DS} , V_{GS} , W , F) while the outputs are small-signal and noise parameters such as transconductance (g_m), output resistance (r_o), minimum noise figure (NFmin), and optimal source conductance (G_{opt}).

The network architecture consists of four hidden layers with 256 neurons each and ReLU activation functions. To embed physical knowledge into the learning process, the total loss function is defined as:

$$L_{total} = L_{data} + \lambda L_{physics}$$

where L_{data} is the mean squared error (MSE) between predicted and simulated parameters, $L_{physics}$ represents the residuals from fundamental transistor equations and λ is a balancing coefficient.

This hybrid formulation enforces physical validity while maintaining learning flexibility. Once trained, the PINN replaces LUTs during design, enabling instantaneous evaluation of device characteristics.

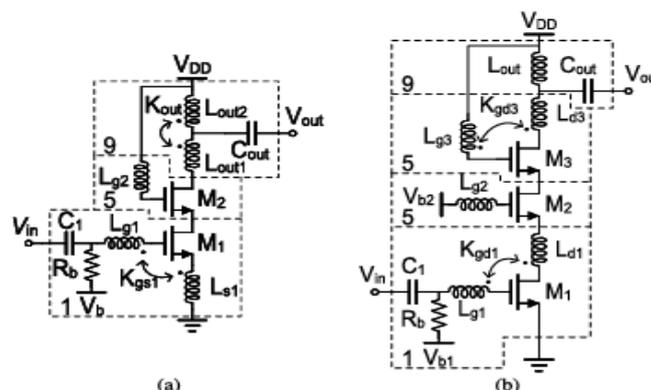


Fig. 3. Low Noise Amplifier based design. (a) Cascode. (b) Stacked.

Reinforcement Learning-Based Topology Generator

The RL topology generator explores the design space by sequentially assembling circuit building blocks into feasible amplifier structures. Each topology is represented as a directed graph, where nodes denote components (transistors, resistors, capacitors, inductors) and edges denote electrical connections.

The RL agent interacts with this environment using a deep Q-network (DQN) policy, where the state S_t represents the current partial circuit, the action A_t defines the next connection or component insertion, and the reward R_t quantifies performance improvement.

The reward function is designed to capture trade-offs among gain, bandwidth, power, and noise figure

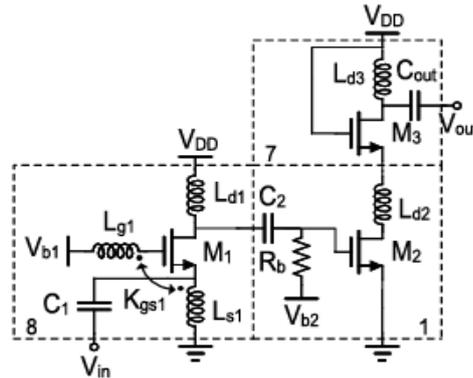


Fig. 4. The Two-Stage gm-Boost LNA

Multi-Objective Optimization and Pareto Evaluation

Once a valid circuit topology is generated, the multi-objective optimization stage determines optimal device sizes and bias conditions. Instead of relying on population-based methods like NSGA-II, a hybrid Bayesian optimization with Pareto front tracking is employed.

The objectives include.

1. Maximization of power gain
2. Minimization of noise figure
3. Minimization of power consumption and
4. Maximization of bandwidth.

Each candidate design xxx is evaluated using the trained PINN model for small-signal parameters and noise behavior. A surrogate Gaussian Process (GP) model predicts the performance distribution and refines the Pareto front iteratively.

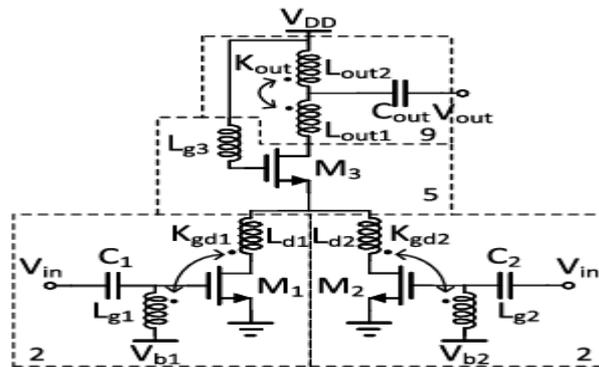


Fig.5. The Dual-Path Noise-Canceling LNA

IV. SIMULATION RESULTS

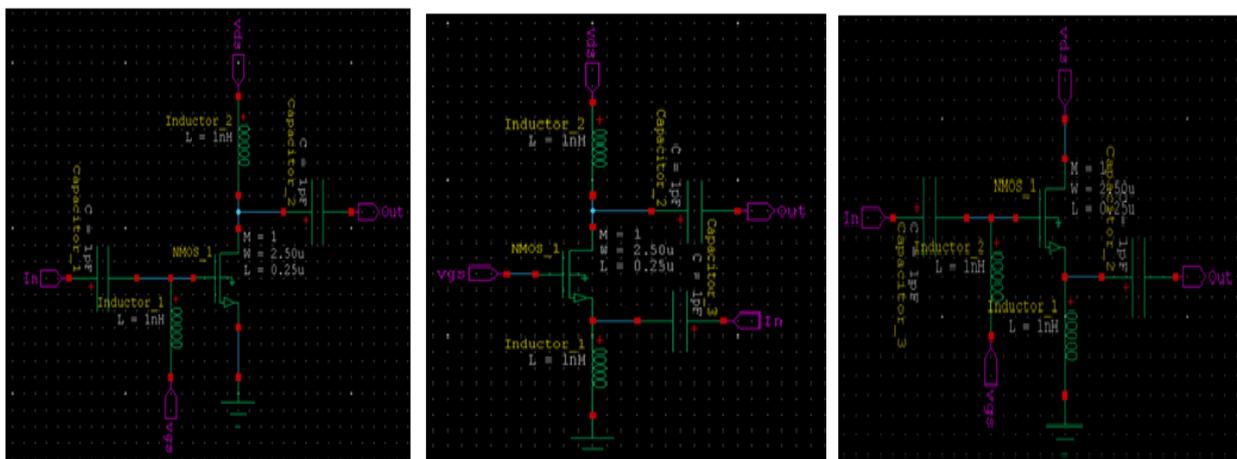


Fig. 6. Schematic Diagrams of CS, CG and CD

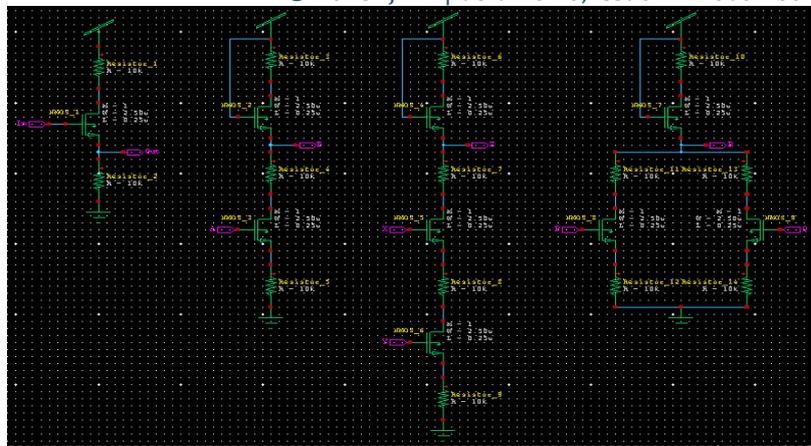


Fig. 7. The Schematic Diagrams of DC topology with (a) one block, (b) two blocks, (c) three blocks and (d) parallel blocks

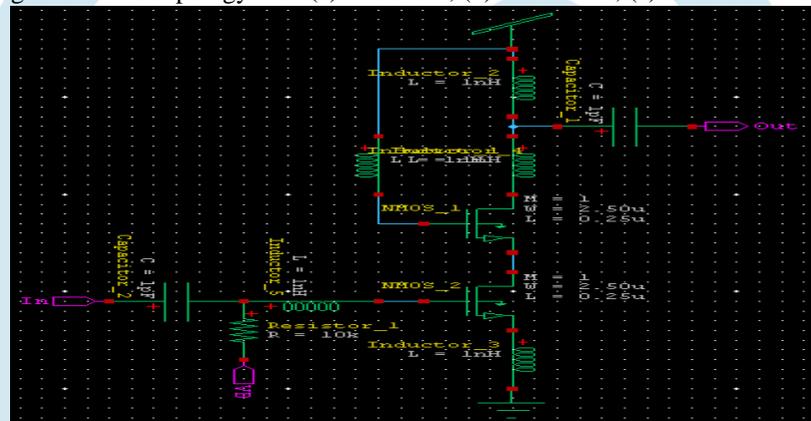


Fig. 8. Schematic Diagram of Low Noise Amplifier based design based on Cascode.

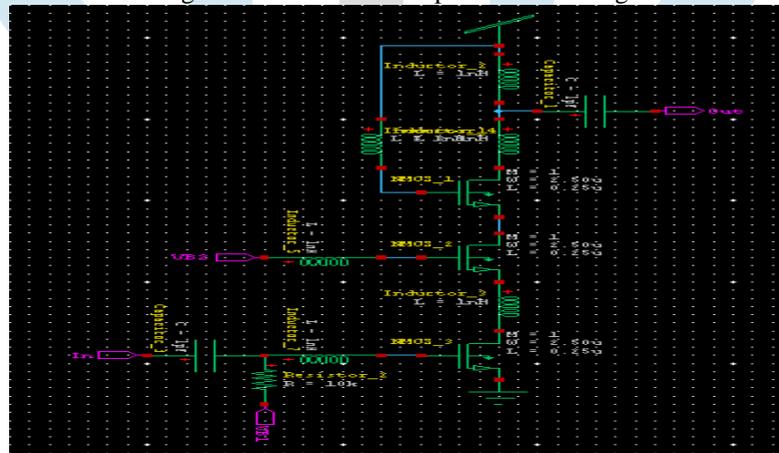


Fig. 9. Schematic Diagram of Low Noise Amplifier based design based on Stacked

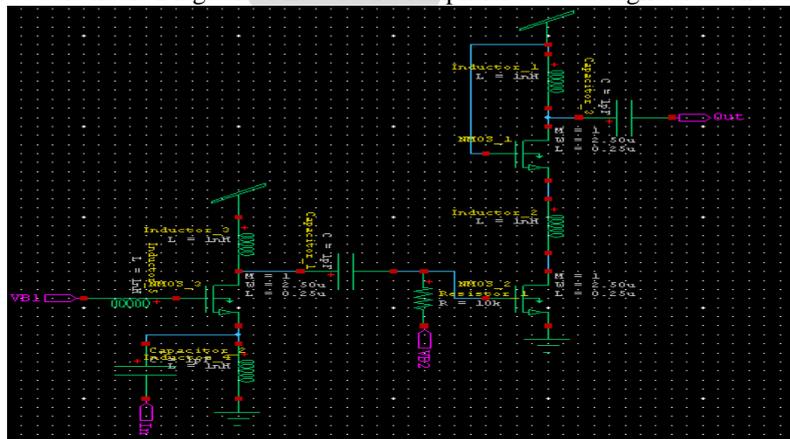


Fig.10. The Schematic Diagram of Two-Stage gm-Boost LNA

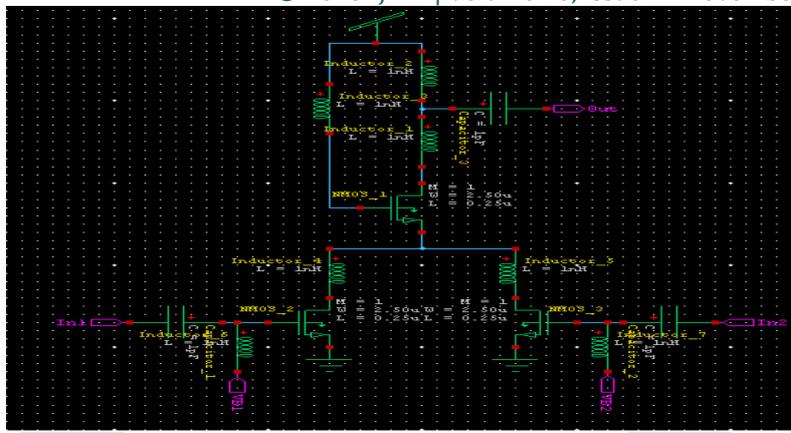


Fig.11. The Schematic Diagram of The Dual-Path Noise-Canceling LNA.

Table 1 Comparison of Optimization Performance

Method	Gain (dB)	NF (dB)	Power (mW)	Time (min)
Low Noise Amplifier based design	21.3	1.48	2.8	79
The Two-Stage gm-Boost LNA	21.8	1.35	3.0	42
Dual-Path Noise-Canceling LNA	22.1	1.27	3.1	22

V. CONCLUSION

The results demonstrate that combining physical priors with data-driven learning provides a more efficient and accurate circuit synthesis process. The framework generalizes across CMOS technologies and can adapt to design constraints without re-training from scratch. Future research will integrate layout-aware modeling, 3D transformer-based passive components, and full schematic-to-layout automation to realize a complete AI-driven RF EDA system. This paper presented an AI-assisted framework for automatic CMOS LNA synthesis using physics-informed neural networks and reinforcement learning. The method unifies topology generation, transistor modeling, and optimization in a single learning loop, significantly reducing design time while maintaining high accuracy. This approach lays the foundation for next-generation AI-enhanced electronic design automation tools for analog and RF circuits.

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