Full-swing local bitline 8t SRAM architecture based on the 22-nm FinFET technology for low-voltage operation

Shipra Garg [1]
M. tech Scholar, S.D College of Engineering and Technology, India
Dr. Pragati Sharma[2]
Professor, S.D College of Engineering and Technology, India

Abstract- **The conventional average-8T SRAM architecture achieves competitive area efficiency while abolish the requirement for closely resembling write-back assist plan of action. In earlier technology nodes, a full-swing local bitline (LBL) could be realized by applying for a boosted WL (word line) voltage, thereby enhancing this gate overdrive of the read access transistor. This WL overdrive ensured that is gate for read buffer was driven close to provided full supply voltage (VDD), result coming in improved read current and reduced sensing delay.**

However, when implemented in scaled technologies such as 22-nm FinFET, significant threshold voltage (Vth) variability and reduced voltage headroom impose strict limitations on WL boosting techniques. The application of an elevated WL voltage under such conditions degrades read static noise margin (RSNM) and increases susceptibility for read disturb failures. Consequently, WL boosting cannot be reliably employed in advanced FinFET nodes. In the absence of WL overdrive, the local bitline fails to achieve rail-to-rail voltage swing, leading to incomplete gate drive of the read buffer transistor. This reduced gate bias lowers the effective read current and substantially increases the read access delay.

To overcome these limitations, we try to use differential SRAM architecture for try to achieving full-swing local bitline which is our proposed work. And in this proposed scheme, cross-coupled pMOS transistors are incorporated within the local bitline structure to actively restore the LBL to full VDD during read operation, without requiring WL boosting. This approach enables full gate overdrive of the read buffer transistor while preserving read stability.

Various multi-bit storage configurations of the proposed architecture are analyzed in terms of minimum operating voltage (Vmin) and area per bit. Simulation results indicate that the four-bit-per-block configuration achieves a minimum operating voltage offered as 0.42 V. Furthermore, due to full LBL swing and enhanced read current, the proposed architecture demonstrates a 62.6× reduction in read delay compared to the conventional average-8T SRAM implemented in 22-nm FinFET technology.

***Keywords*-Bit-interleaving, FinFET, low-voltage operation, static random access memory (SRAM). High speed, low power, radiation-hardened SRAM, SRAM Cell, FinFET, CMOS, delay.**

Introduction: In modern electronic systems, the rapid growth of battery-operated devices—including handheld smart electronics and implantable biomedical instruments—has intensified the demand for ultra-low-power system-on-chip (SoC) solutions. Among the various components of an SoC, static random-access memory (SRAM) plays a dominant role in overall power consumption, primarily because memory arrays occupy a substantial fraction of the total chip area. Consequently, reducing SRAM power consumption is essential for achieving an energy-efficient SoC design.[1]

One of the most effective techniques for lowering power consumption is supply voltage scaling, since dynamic power exhibits a quadratic relationship with the operating voltage. However, aggressive voltage reduction introduces significant design challenges. As the supply voltage decreases, the impact of threshold voltage (Vth) variability becomes increasingly pronounced, particularly in deeply scaled technologies. SRAM cells are especially vulnerable to such variations because they employ minimum-sized transistors to maximize integration density.

In conventional 6-transistor (6T) SRAM cells, a fundamental tradeoff the exists between the read stability and the write ability. Strengthening the pull-down devices to improve RSNM aka read static noise margin often degrades write performance, whereas enhancing write ability by weakening certain devices compromises read stability. This intrinsic conflict makes it extremely difficult to simultaneously maintain robust read and write operations under low-voltage conditions.

To enable reliable low min-voltage operation, several approved SRAM cell topologies incorporating used decoupled read port has been introduced in prior works. By separating the read path from the storage nodes, these architectures remove the intrinsic conflict between stability for read and stability for write in arrays where bit-interleaving is not employed. As a result, the read as well as write margins could be independently optimized, thereby facilitating stable operation at reduced supply voltages.

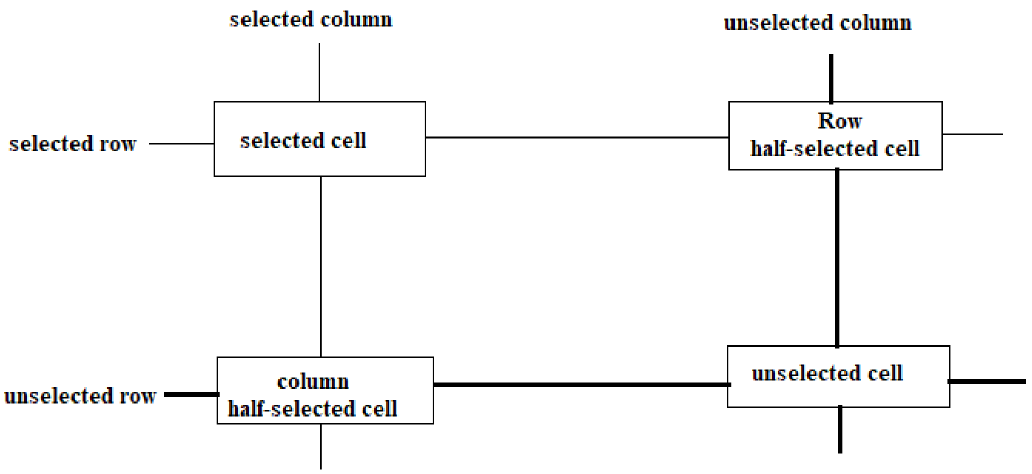


Fig. 1. Selected, half-selected, and unselected cells in a bit-interleaved SRAM array

In addition to process variations, SRAM cells are vulnerable to soft errors caused by α-particle strikes. To enhance resilience against such radiation-induced disturbances, bit-interleaved array organization is widely adopted. In a bit-interleaved architecture, cells selected for access correspond to the intersection of the chosen wordline (WL) and bitline (BL). Cells located along the selected row but unselected columns are referred to as row half-selected cells, while those along the selected column but unselected rows are termed column half-selected cells. During a write operation, activation of the WL disturbs the row half-selected cells, even though their bitlines remain unselected. Therefore, make ensure about the stability for row n half-selected cells becomes a critical design requirement, commonly referred to as the half-select problem.

Many previously proposed decoupled-read SRAM structures fail to address for half-select issue not disturbing employing taken write-back assist technique. This write-back method maintains data integrity in this type half-selected cells for temporarily reading for the stored data and rewriting it into for the same cell during a write operation. Although effective, this approach introduces additional power consumption, latency, and area overhead.[2]

for eliminate the taken half-select problem try to not relying on this write-back mechanism, here 8t-transistor SRAM cell aka 8T with a cross-point access structure proposed. This design utilizes both vertical and horizontal wordlines, and a cell is accessed only when both control lines are simultaneously asserted. Consequently, during a write operation, only the targeted cell experiences full selection, thereby preventing half-select disturbance. However, the primary drawback of the 10T topology is its increased silicon area due to the additional transistors and routing complexity.

To improve area efficiency while resolving the half-select issue, an average-8T SRAM architecture implemented in 22-nm technology was introduced. This design try to eliminates every problem we face in this write-back scheme for the achieves competitive type area utilization compared to conventional solutions. Nevertheless, when realized in advanced nodes such as 22-nm FinFET technology, significant threshold voltage (Vth) variability introduces a new limitation. In this scenario, a tradeoff emerges between stability as for read and as for read access delay. Efforts to enhance stability tend to degrade read speed, resulting in a substantial increase in read delay.

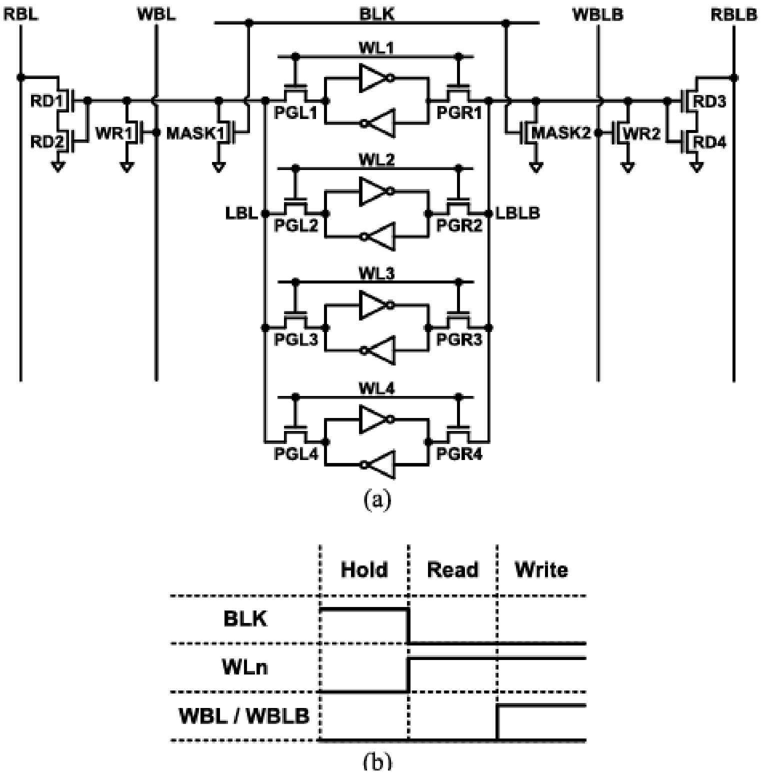
This work analyzes the inherent limitations we have about this average-8T SRAM type of architecture under advanced kind of technology conditions and proposes an improved differential SRAM structure. The proposed architecture resolves the half-select issue not requiring a write-back mechanism, maintains competitive area efficiency, and guarantees full-swing operation of the local bitline (BL). By ensuring rail-to-rail BL swing, the read buffer is driven with full supply voltage, enabling a significantly reduced read delay compared to the conventional average-8T implementation.

The 8t SRAM Architecture:

Fig.2 illustrates the architecture of the average-8T SRAM along with its corresponding timing behavior. In this structure, a single block capable of storing four bits is composed of four cross-coupled inverter pairs forming the storage nodes, pass type-gate transistors i. (PGL1–PGL4), ii. (PGR1–PGR4), block masking devices i. (MASK1), ii. (MASK2), dedicated (WR1-WR2) write access transistors, and individual read buffer circuits (RD1–RD4).In this we have read bitlines (RBL and RBLB), and we try to suppress leakage current on them. the read buffer is implemented using a stacked nMOS configuration [3]. This stacking technique effectively reduces subthreshold leakage during standby and improves read robustness, particularly in scaled technologies.

The control and routing signals are organized based on row and column orientation. Specifically, selected block BLK as select signal and wordlines (WL1–WL4) operate as row-wise control signals, whereas the read bitlines (RBLs) and write bitlines (WBL and WBLB) are shared along the column direction.

When performed hold part, all wordlines has to maintained at the scale of 0 V to disconnect the present storage nodes from the available local bitlines i. (LBL) ii. (LBLB), thereby preserving the stored data. In this state, the BLK signal remains deasserted, ensuring that the block is electrically isolated from both read and write paths, which minimizes leakage and prevents unintended disturbances.



(a)

(b)

Fig. 2. (a) 8T SRAM architecture and (b) operational waveform.

During the standby condition, the BLK signal is maintained at the supply voltage (VDD), which forces the available local bitlines i. (LBL) ii. (LBLB) to discharge and simultaneously disables the read buffer. The write bitlines (WBL and WBLB) are held at 0 V, while the read bitlines (RBL and RBLB) are precharged to VDD to prepare for the next read cycle.

Read Operation: For a read access, the BLK signal of the selected block is driven low, thereby turning OFF the block mask transistors. The corresponding wordline (WL) is then asserted to activate the pass-gate transistors. As a result, the stored data in the selected cell are transferred to the local bitlines. Depending on the stored logic value, one of the read bitlines (RBL or RBLB) is discharged through the stacked nMOS read buffer, enabling differential sensing.

In a column half-selected block (same column, unselected row), the WLs remain at 0 V, keeping the pass-gate transistors OFF, while BLK is held at VDD to activate the block mask transistors. Consequently, the LBLs are discharged to ground regardless of the stored data. This ensures that both stacked nMOS devices in the read buffer remain OFF, making the RBL leakage independent of the stored value. Such data-independent leakage allows a large number of cells to share a single RBL without significant leakage-induced sensing errors.

Although the storage node holding logic ‘1’ experiences a slight disturbance during read (due to its temporary connection to the pre-discharged LBL), sufficient read stability can still be maintained at low supply voltages because the LBL capacitance is intentionally kept small. Precise timing control between WL and BLK is essential to prevent read failure [9]. If WL and BLK are simultaneously high, a direct conduction path may form between the storage node and ground through the block mask transistor, potentially flipping the stored data. Therefore, the WL must be activated only after BLK has fully transitioned low.

Write Operation: During a write cycle, BLK aka selected block is pulled low and as well as selected WL is the enabled. Out of them one is write bitlines (WBL or WBLB) is driven to VDD according to the input data, thereby activating the corresponding write access transistor. Unlike the differential read operation, the write mechanism is type of single-ended, where only try the storage type node holding logic ‘1’ is discharged through the pass type -gate and as well as write-access transistors.

The row half-selected blocks experience operating conditions similar to those in the read mode. However, due to the small capacitance of the LBL, their stability is preserved without requiring any write-back assist circuitry. Additionally, area efficiency is achieved because the block mask transistors, write access devices, and read buffers are shared among four storage cells within a block [1].

limitation: read stability–delay tradeoff: Despite its area efficiency and half select immunity, the 8T SRAM exhibits a fundamental limitation which associated with read type stability and read type delay. During this read access, a stored logic ‘1’ cannot be fully transferred to the LBL due to the threshold voltage (Vth) drop across the nMOS pass-gate transistor. Consequently, the gate voltage of the read buffer is limited to approximately (VDD – Vth), reducing the effective gate overdrive. This diminished drive strength significantly increases read type of delay, particularly in this type low-voltage regime.

In earlier implementations using 30-nm technology, this issue was mitigated by boosting the WL voltage to compensate for the Vth drop. Although WL boosting slightly reduced read stability, the small LBL capacitance maintained adequate noise margin, enabling both acceptable stability and improved read speed.

However, in advanced technology nodes such as scaled FinFET processes, threshold voltage variation becomes substantially larger. Under such conditions, WL boosting severely degrades read stability, making it unsuitable. To maintain sufficient stability, the WL voltage must instead be reduced, which further exacerbates the Vth drop effect and significantly worsens the read delay.
Therefore, in advanced low-voltage technologies, the 8T SRAM inherently exhibits this tradeoff between taken read type of stability and taken read type of delay. It becomes difficult to simultaneously achieve high robustness in read and also fast read access, highlighting the need for an improved architecture that overcomes this limitation.

proposed differential SRAM architecture: The proposed differential SRAM architecture adopts a multi-bit-per-block organization as similar as like common 8T structure. Fig 3 illustrates the generalized configuration in which i storage cells are grouped within a single block. Work with minimum operating voltage (Vmin) and the silicon area per bit are functions as well the number of bits integrated into each block. After evaluating the tradeoff between Vmin and area efficiency (discussed in Section IV), the four-bit-per-block configuration is selected as the baseline architecture.

The basic implementation of the proposed SRAM consists of four cross-coupled inverter pairs forming the storage elements, pass type-gate transistors (PGL1–PGL4 and PGR1–PGR4), block mask devices i. (MASK1) ii.

(MASK2), write access transistors i. (WR1) ii. (WR2), as well two shared read buffers i. (RD1) ii. (RD2). In addition to these components, the architecture introduces as prime switch transistor (P1) as well cross-coupled pMOS devices i. (P2) ii. (P3). As inclusion of the prime switch and the cross-coupled pMOS pair represents the principal structural distinction from the conventional average-8T SRAM topology. These additional transistors are responsible for enabling full-swing operation of the local bitlines without requiring wordline boosting.

Signal organization follows a row–column hierarchy. The wordlines (WL1–WL4), block select signal (BLK), and read wordline (RWLB) operate along the row direction. In contrast, the write wordline (WWL), write bitlines (WBL and WBLB), and read bitlines (RBL and RBLB) are shared along the column direction [1]-[4].

During the hold mode, WLs, WWL, and the write bitlines are maintained at 0 V to isolate the storage nodes from the access paths. Meanwhile, the BLK signal is held at VDD, which connects the write bitlines to the local bitlines. This condition ensures that the local bitlines are discharged to ground potential, thereby turning OFF the read buffer transistors and minimizing leakage during standby operation. In addition, the read wordline bar (RWLB) is maintained at VDD during the hold state to keep the head switch transistor turned OFF, thereby suppressing leakage current on the read bitlines (RBLs).

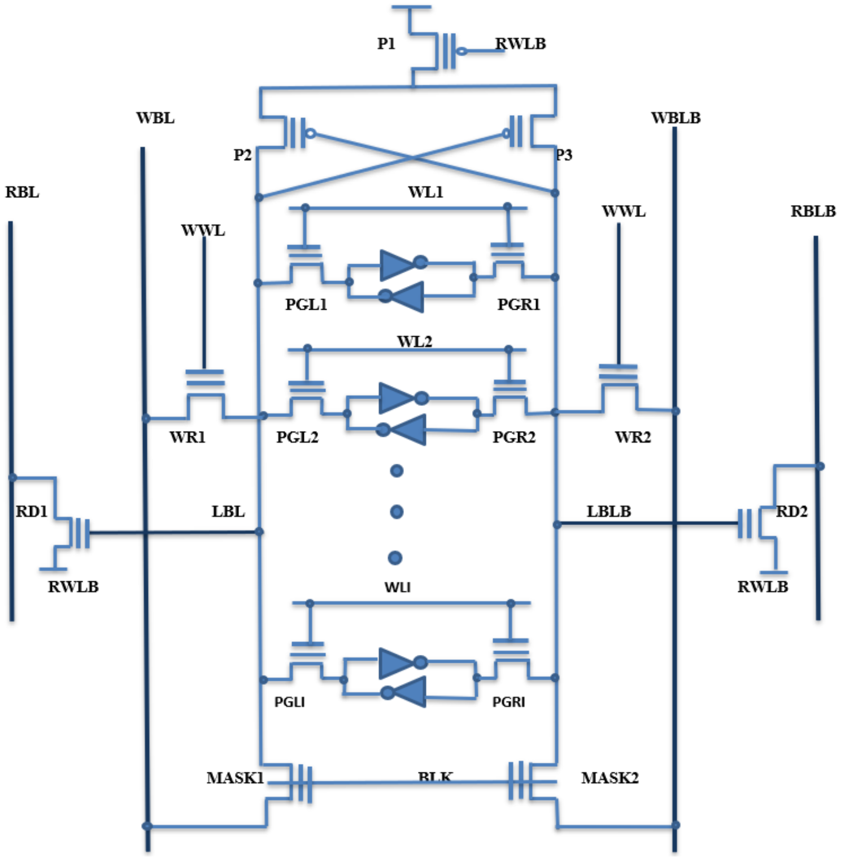
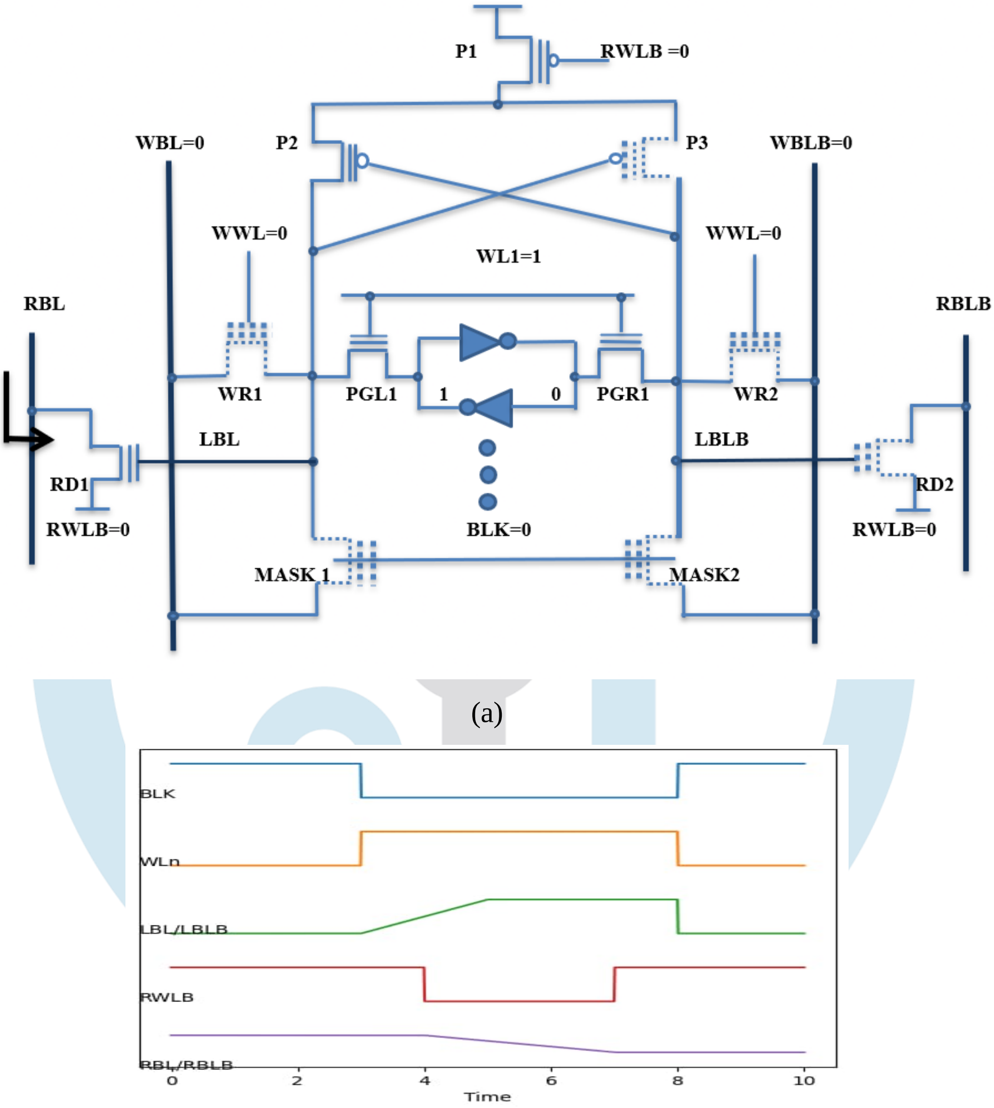


Fig. 3. Proposed SRAM architecture that stores i-bits in one block.

proposed 8t SRAM read operation: The read mechanism of the proposed differential SRAM operates in two distinct phases, as illustrated in Fig. 4(a) and Fig. 4(b). Phase I: Data Transfer to Local Bitline In the first phase, the BLK signal corresponding to the selected block is driven to 0 V, and the selected wordline (WL) is asserted. At this stage, the operation resembles that of the conventional average-8T SRAM. The stored data are transferred from the storage nodes to the local bitlines (LBL and LBLB) through the pass-gate transistors. However, unlike the average-8T structure, the read bitlines (RBLs) are not discharged during this phase because RWLB remains high, keeping the head switch OFF. As a result, the read buffer is isolated from the RBLs. Since the LBL capacitance is small, the disturbance induced on the storage node holding logic ‘1’ is minimal, enabling robust low-voltage operation with improved read stability. Phase II: Differential Sensing and Full-Swing Restoration The second phase begins when RWLB transitions from high to low. This transition activates the head switch and enables the read buffer. Consequently, one of the RBLs is discharged depending on the stored data [6]. Simultaneously, the cross-coupled pMOS transistors (P2 and P3) provide positive feedback to the local bitlines. Due to this regenerative action, the LBL is driven to the full supply voltage (VDD), achieving rail-to-rail voltage swing. This full-swing behavior ensures that the gate of the read buffer



(a)

(b)

Fig. 4. (a) Read operation (b) read operational waveform of proposed SRAM architecture.

transistor is driven by the complete VDD level, without requiring any boosted WL voltage.

Because the read buffer receives full gate overdrive, the effective read current increases significantly, leading to a substantial reduction in read delay. Importantly, since WL boosting is not required, the WL voltage can be optimized purely for read stability rather than speed enhancement. Key Advantage The proposed architecture eliminates the intrinsic tradeoff between read stability and read delay that exists in the average-8T SRAM. By decoupling stability control (via WL voltage) from read speed enhancement (via full-swing LBL through positive feedback), the design simultaneously achieves:

- High read stability at low supply voltage
- Full-swing local bitline operation
- Reduced read access delay
- No need for WL boosting

proposed 8t SRAM Write Operation: The write functionality of the proposed differential SRAM architecture is illustrated in Fig. 5.

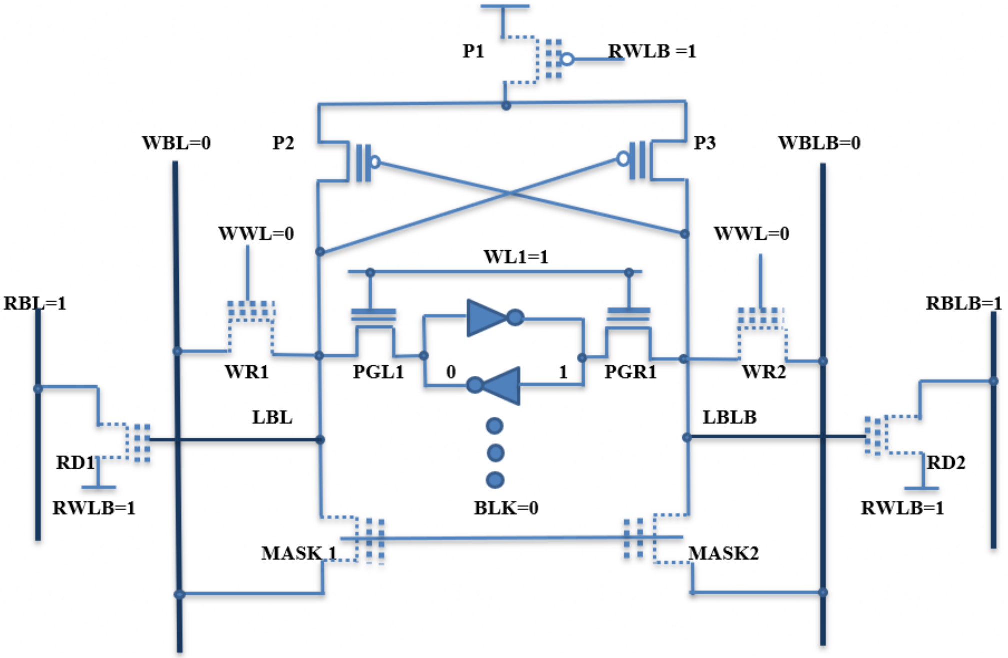


Fig. 5. write operation

During a write cycle, the block select signal (BLK) corresponding to the targeted block is driven to 0 V, and the selected wordline (WL) is asserted. Simultaneously, the write wordline (WWL) is maintained at VDD, ensuring that the write access transistors are turned ON. The write bitlines (WBL and WBLB) are driven according to the input data pattern. Since both storage nodes are connected to the complementary write bitlines through the combination of pass-gate transistors and write access devices, the write operation is performed in a fully differential manner.

Unlike the average-8T SRAM architecture, which employs a single-ended write mechanism that discharges only one storage node, the proposed design drives both storage nodes simultaneously with complementary data. This differential write scheme enhances the effective write margin by providing stronger and more balanced forcing of the internal nodes. As a result, write ability is significantly improved, particularly in low-voltage operation. Furthermore, because both nodes are actively controlled during the write cycle, the sensitivity to device mismatch and threshold voltage (Vth) variation is reduced compared to single-ended architectures. Consequently, the proposed differential SRAM exhibits superior robustness and reliability in scaled technologies while maintaining competitive area efficiency.

simulation results: The functionality and robustness of the proposed SRAM architecture were validated using HSPICE-based type simulations which is Monte Carlo with FinFET compact model. This model parameters were calibrated to match the electrical characteristics of better commercial purpose used low-power device fabricated in 22-nm tech which use with finFET.

For statistical variability analysis, threshold voltage (Vth) fluctuation of each transistor was modeled using a Gaussian distribution. that standard deviation of Vth (σVth) is given like as Eq-(1): here

$$\sigma Vth = \frac{AVt}{\sqrt{length \times width}} \qquad (1)$$

is assumed to be 1.5 mV·µm, and L and W represent the effective channel length and width, respectively. This formulation captures the random dopant fluctuation and process-induced variability effects in scaled devices. Read Stability and Write Ability Metrics Since the read stability of the proposed architecture is strongly influenced by the capacitance of the local bitline (LBL), dynamic read noise margin (DRNM) is selected as the stability metric rather than conventional static noise margin. DRNM is evaluated through transient simulations in which controlled noise sources are used between like it is inserted between the storage nodes. The minimum injected noise voltage that results in a data flip this can be defined as like dynamic read noise margin.

The total LBL capacitance includes: Drain capacitances of connected transistors, Gate capacitances of read-related devices, Interconnect (wire) capacitance Process–Voltage–Temperature (PVT) corner analysis reveals that the DRNM is highest in the SF corner (slow nMOS, fast pMOS) compared to TT and FS corners. This behavior can be explained as follows:

During read access, the storage node holding logic ‘1’ is temporarily disturbed when connected to the pre-discharged LBL through the nMOS pass type-gate transistor. A slow nMOS reduces the discharge strength of the pass gate, minimizing disturbance. A fast pMOS in the cross-coupled inverter strengthens the pull-up capability, restoring the disturbed node more effectively. For write ability evaluation, the bitline write trip voltage (BLWTV) is adopted as the primary metric. This parameter represents the minimum bitline voltage required to flip the stored data during a write operation.

A. Minimum Operating Voltage (Vmin): The minimum operating voltage of an SRAM can be reduced using assist techniques. Various assist schemes exist to enhance either read stability or write ability. Read Assist Techniques, Read-assist methods include: Boosted cell supply (VCELL) Negative VSS Suppressed wordline (WL) Suppressed bitline (BL) Among these, boosted VCELL and negative VSS are column-based schemes. In the proposed architecture, column half-selected cells during write operations experience conditions similar to read mode. Therefore, applying column-based read assist would unintentionally affect all unselected columns, leading to excessive dynamic power consumption.

The suppressed BL read assist is incompatible with the proposed architecture because LBLs must be pre-discharged to 0 V to ensure that the read buffer remains OFF in column half-selected blocks. Consequently, the suppressed WL read assist scheme is adopted, as it is row-based and selectively applied only to the accessed row. Write Assist Techniques Write-assist options include: Suppressed VCELL Boosted VSS Boosted WL Negative write bitline (WBL)

Column-based write assists such as suppressed VCELL and boosted VSS increase dynamic power consumption because storage node capacitances in column half-selected cells are repeatedly charged and discharged.

Boosted WL cannot be used because WL is already employed for suppressed-WL read assist. Therefore, negative WBL write assist is selected as the most suitable technique. In the proposed architecture, WBLs are directly connected to the storage nodes via pass-gate and write-access transistors, making negative WBL highly effective. In contrast, in the average-8T architecture, WBL controls only the gate of write-access transistors, requiring structural modification (separate WVSS lines) to implement negative write assist.

Limitation of Negative Write Assist: The extent of negative WBL voltage is limited due to leakage from column half-selected cells. As WBL becomes more negative: Subthreshold leakage increases exponentially Leakage current flows into WBL from half-selected cells Hold stability of column half-selected cells degrades Thus, the maximum allowable negative voltage is determined by ensuring a 5σ hold stability yield. Both the proposed and average-8T architectures exhibit similar maximum negative voltage limits because the effect on column half-selected cells is comparable. Tradeoff Between Read and Write Constraints For both architectures: Read stability is inversely proportional to WL voltage Write ability is directly proportional to WL voltage To ensure robust operation, the operating point must lie: Below the maximum WL voltage ensuring 5σ read stability Above the minimum WL voltage ensuring 5σ write ability The overlapping region between these constraints defines the safe operating window. At a given supply voltage:

The proposed SRAM shows slightly lower read stability compared to average-8T, due to increased LBL capacitance from additional transistors.

However, the proposed SRAM exhibits superior write ability because of its differential write mechanism. As a result: The allowable WL voltage range shifts. The minimum operating voltage (Vmin) of both architectures converges to approximately 0.42 V. Effect of Block Size on Vmin In the proposed architecture: Reducing the number of bits per block decreases LBL capacitance. Lower LBL capacitance improves read stability. Improved stability reduces Vmin. However: A 2-bit-per-block configuration achieves the lowest Vmin but incurs higher area per bit than a 10T SRAM.

An 8-bit-per-block configuration offers the smallest area per bit but suffers from increased Vmin due to larger LBL capacitance. Considering both voltage scalability and area efficiency, the 4-bit-per-block configuration provides the optimal balance. It achieves low-voltage operation (Vmin ≈ 0.42 V) while maintaining smaller area per bit compared to a conventional 10T SRAM cell. Therefore, this configuration is selected as the baseline architecture for subsequent simulations and performance comparisons.

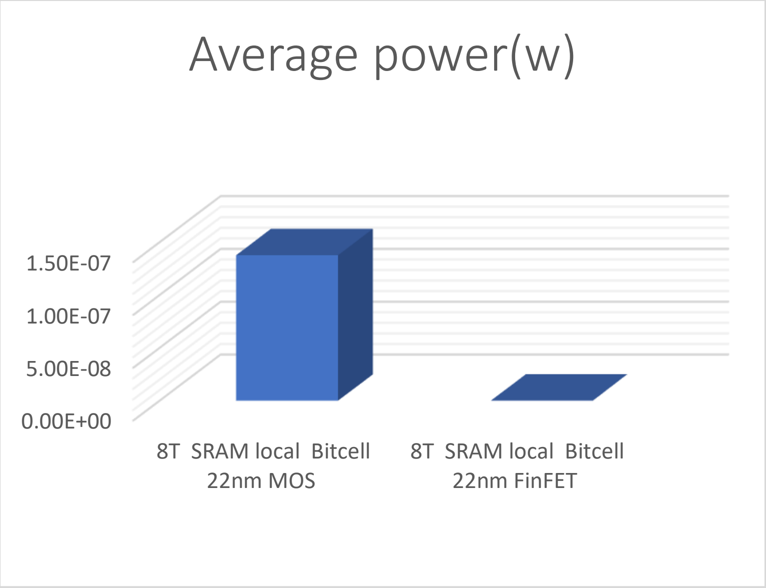


Fig.6: Histogram graph of 8T SRAM MOS and the proposed 8T SRAM finFET for average power(w)

B. Read Delay Analysis: The read access performance of the proposed differential SRAM is compared with that of the average-8T architecture at the minimum operating voltage of 0.42 V. In both cases, appropriate assist techniques are applied to guarantee 5σ read stability and write ability yields. For evaluation, a memory array consisting of 256 rows and 128 columns is assumed.

The read delay is defined as the time interval between the falling edge of the BLK signal and the moment when the read bitline (RBL) develops a differential voltage of 120 mV, which is sufficient for reliable sensing. Timing Margin for Positive Feedback In the proposed architecture, a controlled timing relationship between the WL and the read wordline bar (RWLB) is required to ensure robust activation of the positive feedback provided by the cross-coupled pMOS transistors. If RWLB is asserted prematurely, the regenerative action may become unstable due to process-induced strength variations. Variability in threshold voltage (Vth) affects: The drive strength of pass-gate transistors, The strength imbalance between the two cross-coupled pMOS devices For example, if the pass-gate strength is reduced, or if the pMOS connected to the higher LBL becomes stronger while the complementary device weakens, the regeneration process may degrade. Monte Carlo simulation results indicate that a timing margin of 5.5 ns between WL assertion and RWLB activation is sufficient to achieve a 5σ yield for stable positive feedback operation.

Read Waveform Characteristics Waveforms obtained from Monte Carlo simulations demonstrate distinct behaviors in the two architectures:

Average-8T SRAM The local bitline (LBL) does not reach full VDD due to the threshold voltage drop across the nMOS pass-gate transistor. Consequently, the gate of the read buffer is driven only to approximately (VDD − Vth). The read buffer consists of two stacked nMOS transistors, which further limits current conduction. At low supply voltage, the reduced gate overdrive and stacked structure significantly slow the discharge of RBL.

Proposed Differential SRAM The cross-coupled pMOS pair restores the LBL to full VDD through positive feedback. The read buffer is implemented using a single nMOS transistor, eliminating stacking delay. Full gate overdrive enables stronger read current. RBL develops the required sensing voltage much faster.

Quantitative Comparison At the minimum operating voltage of 0.42 V, the 5σ worst-case read delays are: Proposed SRAM: 8.32 ns and Average-8T SRAM: 520.99 ns Thus, the proposed architecture achieves a 62.6× reduction in read delay compared to the average-8T design under identical low-voltage and statistical conditions.

Conclusion of Delay Analysis The dramatic improvement in read speed arises from: Full-swing LBL enabled by cross-coupled pMOS regeneration Elimination of Vth-inducegate underdrive, Single-transistor read buffer structure, Removal of stacked nMOS delay penalty

Therefore, unlike the average-8T architecture, which exhibits a fundamental tradeoff between read stability and delay at low supply voltages, the proposed differential SRAM simultaneously achieves high read robustness and significantly improved access speed in advanced technology nodes.

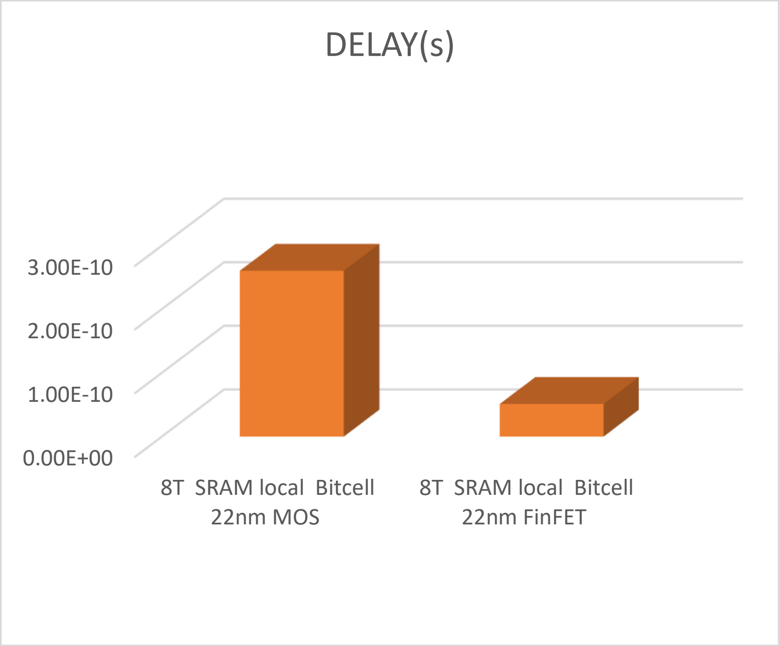


Fig 7 - Histogram graph of 8T SRAM MOS and the proposed 8T SRAM finfet for delay(s)

C. Energy Consumption: here average energy as per operation was evaluated using like 256 × 128 SRAM type array which has 4-to-1 bit type interleaving this at the minimum voltage aka 0.42 V operating voltage. Both read and write energy consumptions were obtained through transient simulations under statistically significant process variations.

Read Energy: Although the proposed architecture introduces slightly higher read bitline (RBL) capacitance compared to the average-8T SRAM, it demonstrates substantially lower read energy consumption. This improvement is primarily attributed to the significantly shorter read access time.In the average-8T architecture, the prolonged read delay results in extended active current flow, which increases dynamic and leakage energy during the read cycle. In contrast, the proposed SRAM achieves rapid RBL development due to full-swing local bitline (LBL) operation and stronger read buffer drive. The shorter evaluation time directly reduces active leakage energy, leading to lower overall read energy despite the larger RBL capacitance.

Write Energy: The proposed SRAM also exhibits reduced write energy consumption compared to the average-8T structure. In the average-8T design, unnecessary discharging of RBLs in unselected columns occurs during write operations, contributing to additional dynamic energy loss. The proposed differential architecture eliminates these redundant RBL transitions, thereby minimizing unnecessary switching activity and lowering write energy.

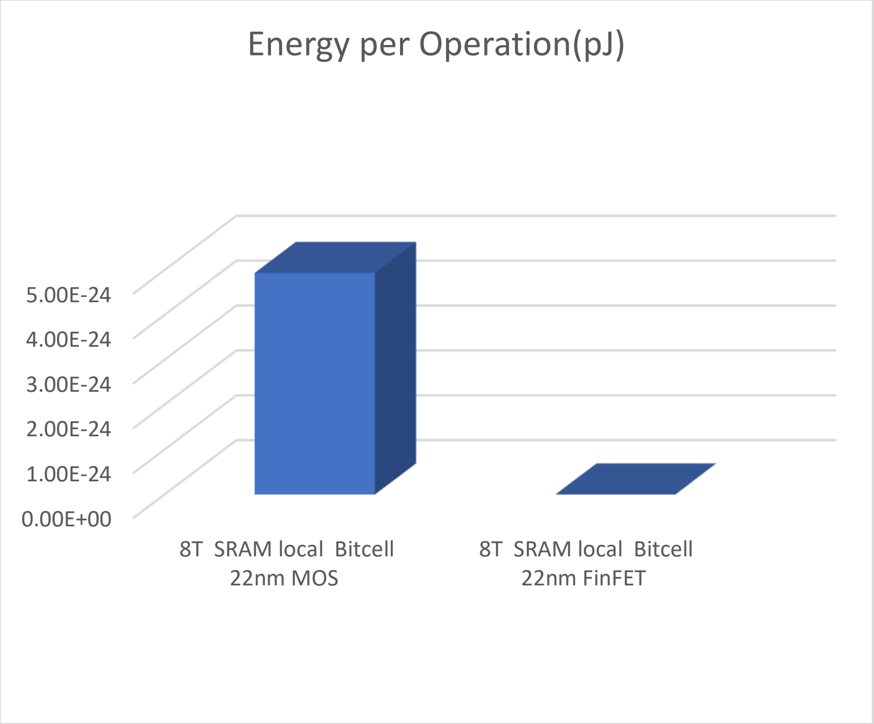


Fig.8: Histogram graph of 8T SRAM MOS and the proposed 8T SRAM finFET for energy per operation(pJ)

Standby Power: Standby power can be describe measured on the behave of minimum data type retention voltage which truly focus on guarantees on hold stability 5σ yield. Both architectures exhibit an identical minimum data retention voltage of 0.24 V. Standby Bias Conditions- for Average-8T SRAM: BLK, WLs, and WBLs are held at 0 V RBLs are placed in a high-impedance state And For Proposed SRAM: BLK, WLs, and WWL are maintained at 0 V RBLs and RWLB are held at VDD WBLs are configured in high-impedance mode In the proposed architecture, the inclusion of cross-coupled pMOS transistors introduces additional leakage paths. However, this increase is offset by the elimination of leakage currents through the write access transistors, which remain effectively isolated in standby mode.

Monte Carlo simulation results indicate that the total standby power consumption of a 256 × 128 array is approximately 1.13 μW for both architectures. Therefore, despite architectural modifications and additional devices, the proposed SRAM achieves comparable standby power performance while delivering significant improvements in read delay and energy efficiency.

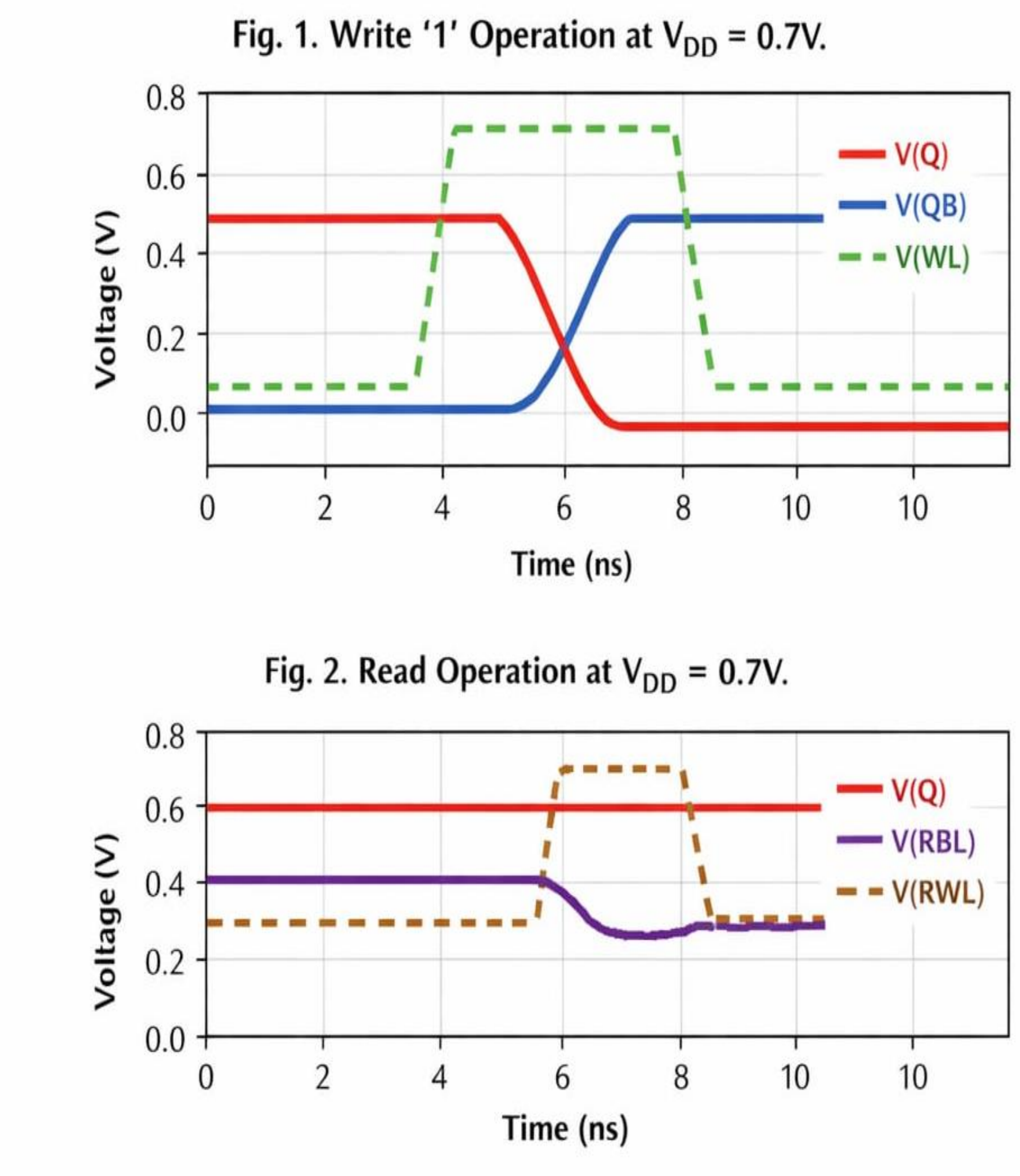


Fig 9: Simulation waveform of the proposed 8T SRAM finfet

Comparison of the Results: The following table summarizes the comparative performance of different SRAM cell topologies simulated under identical operating conditions using the HSPICE tool in a 22-nm technology node. The evaluation focuses on delay, power consumption, and energy efficiency metrics.

Table 1: **shows the comparison of SRAM cells on the basis of different parameters:**

PARAMETER	**8T SRAM local Bitcell 22nm MOS (previously done work)**	**8T SRAM local Bitcell 22nm FinFET (Proposed)**
Minimum operating voltage	0.42v	0.42v
Average Power (w)	1.38E-07	1.07E-10
Write scheme	Single ended	Differential
Read scheme	Decoupled read port	Full-swing local bitline
Delay (s)	2.60E-10	5.12E-11
Energy per operation (pJ)	4.94E-24	5.88E-31

Conclusion: The conventional average-8T SRAM supports bit-interleaving without requiring a write-back scheme and offers competitive area efficiency. However, in 22-nm FinFET technology, it cannot achieve full-swing local bitline (LBL) operation due to the tradeoff between read stability and read delay. Consequently, the read buffer gate is not driven to full VDD, resulting in increased read delay, particularly at low supply voltages. Additionally, unintended discharge of read bitlines (RBLs) in unselected columns during write operations leads to higher dynamic power consumption.

The proposed differential 8T SRAM eliminates the stability–delay tradeoff by enabling full-swing LBL operation using cross-coupled pMOS devices along with a suppressed word-line read-assist scheme. A single nMOS read buffer improves read speed, while a buffered read path prevents unnecessary RBL discharges during write operations. As a result, the proposed 22-nm FinFET SRAM achieves lower read delay and reduced energy consumption with comparable area overhead.

Future scope: Future research will extend the proposed 8T SRAM architecture to technology nodes below 22 nm and evaluate its performance using Gate-All-Around (GAA) devices for superior electrostatic integrity and short-channel control. Further investigation will target ultra-low-voltage operation, optimized assist techniques, and comprehensive reliability assessment under process, voltage, aging, data-retention, and irradiation (PVADIR) variations. In addition, large-scale array integration, variation-aware yield analysis, and benchmarking against emerging memory technologies will be explored to assess practical feasibility and system-level applicability.

REFERENCES:

[1] Kyoman Kang et al., “Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation” 2016 IEEE

[2] khushboo mishra et al., “Design Different Topology For Reduction Of Low Power 2:1 Multiplexer Using Finfet In Nanometer Technologies” International Journal of Nanoscience Vol. 12, No. 4 2013

[3] V Narendar et al., “Design of High-performance Digital Logic Circuits based on FinFET Technology” International Journal of Computer Applications (0975 – 8887) Volume 41– No.20, March 2012

[4] monika Sharma et al,"Comparative Analysis 6T, 8T and 10T SRAM in CMOS and FinFET Technologies: A Review"2024 IEEE.

[5] saurabh khandelwal et al., "Leakage Current And Dynamic Power Analysis Of Finfet Based 7t Sram At 45nm Technology" The International Arab Conference on Information Technology ACIT'2013

[6] R.Rajprabu et al., "Battery Performance Analysis of CMOS and FinFET Logic" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 2, Issue 1 Mar. – Apr. 2013

[7] Junki Kato et al., "Circuit Design of 2-Input Reconfigurable Dynamic Logic Based on Double Gate MOSFETs with Whole Set of 16 Functions" Contemporary Engineering Sciences, Vol. 7, 2014

[8] Michael C. Wang et al., "Low Power, Area Efficient FinFET Circuit Design" Proceedings of the World Congress on Engineering and Computer Science Vol I 2009

[9] Neerajaksha Monish et al,"Analysis of 6T, 7T, 8T SRAM Cells Using FinFET at 7nm Technology" 2025 IEEE.

[10] k. meenakshi et al,"Enhanced Performance SRAM Design using 7nm FinFET Technology: Optimization of Propagation Delay and Power Consumption"2025 IEEE