Design and Performance Analysis of Multi-Digit BCD Adder Using Brent–Kung Architecture

K.Rojamani[1], S.Praneeth Sai[2], B.Hanumantha Rao[3] , Y.V.V.S.N.Manikanta[4]
[1]Assistant Professor, Dept of ECE, Krishna University College of Engg & Tech, Machilipatnam, AP, India
[2,3,4]UG Students, Krishna University College of Engg & Tech, Machilipatnam, AP, India

ABSTRACT

The design of high-speed and power-efficient arithmetic units is a critical requirement in modern VLSI systems, particularly for applications that demand accurate decimal computations such as financial processing and digital signal processing. This work presents an optimized multi-digit Binary Coded Decimal (BCD) adder based on a parallel prefix structure using the Brent–Kung Adder (BKA), and compares its performance with a conventional Carry Lookahead Adder (CLA) based design.

The proposed and existing architectures are implemented for multiple digit configurations and evaluated in terms of delay and power consumption. The results indicate that the proposed BKA-based BCD adder achieves a significant reduction in delay of approximately 32% for lower digit designs and about 22% for higher digit designs. Similarly, power consumption is reduced by around 7% for smaller configurations and up to 10% for larger configurations when compared to the conventional CLA-based approach. These improvements are attributed to the reduced logic depth and efficient carry propagation mechanism of the Brent–Kung architecture. Furthermore, the proposed design demonstrates better scalability with increasing digit size, making it highly suitable for high-performance and low-power VLSI applications.

Keywords: VLSI Architecture**,** BCD addition, Carry look ahead, Brent kung and Verilog HDL.

I. INTRODUCTION

Binary Coded Decimal (BCD) adders are fundamental components in digital systems that require accurate decimal arithmetic, such as financial processing, commercial computing, and digital signal processing applications. Unlike binary adders, BCD adders represent each decimal digit separately using a 4-bit code, ensuring precise decimal calculations without conversion errors. However, achieving high speed and low power consumption in multi-digit BCD addition remains a significant challenge, especially as the operand size increases. Traditional designs such as ripple carry adders suffer from large propagation delays due to sequential carry transmission, which limits their performance in high-speed VLSI systems.

To overcome these limitations, faster adder architectures like the Carry Lookahead Adder (CLA) have been widely used as the existing solution for BCD addition, offering improved speed through parallel carry generation. However, CLA-based designs introduce increased complexity, higher power consumption, and scalability issues for large digit widths. In this context, parallel prefix adders such as the Brent–Kung Adder (BKA) provide an efficient alternative by reducing logic depth and

optimizing carry propagation. This work focuses on the design and analysis of a multi-digit BCD adder using the Brent–Kung architecture and presents a comparative study with the conventional CLA-based design, demonstrating improvements in delay, power consumption, and scalability for high-performance VLSI applications.

II. LITERATURE SURVEY

The development of efficient Binary Coded Decimal (BCD) adders is closely linked to the evolution of decimal arithmetic in digital systems. Early work by Mike F. Cowlishaw [3] laid the foundation for decimal floating-point algorithms, emphasizing the need for precise decimal computations in financial and commercial applications. Traditional BCD adder implementations primarily relied on ripple carry adders, which suffer from significant delay due to sequential carry propagation. To overcome this limitation, faster architectures such as Carry Lookahead Adders (CLA) were introduced, improving speed through parallel carry generation. Further improvements in logic design, including the use of three-input XOR and majority gates, have been proposed to enhance the performance and efficiency of BCD adders [2].

With the increasing demand for high-performance arithmetic units, researchers have explored advanced hardware implementations and optimization techniques. For instance, high-frequency decimal multipliers have been developed to support faster arithmetic operations in modern processors [4]. Power-efficient design approaches for decimal arithmetic units have also been investigated, focusing on reducing switching activity and optimizing circuit structures to minimize energy consumption [5].

III. METHODOLOGY

32-DIGIT BCD ADDER USING BRENT–KUNG ADDER (BKA)

The proposed methodology focuses on the design and implementation of a high-speed and power-efficient 32-digit Binary Coded Decimal (BCD) adder using the Brent–Kung Adder (BKA) architecture. In this design, each decimal digit is represented using a 4-bit BCD format, resulting in a total of 128 bits for 32-digit inputs. The addition process is carried out in two stages at each digit level. First, binary addition of corresponding 4-bit digits along with carry-in is performed using the Brent–Kung parallel prefix adder, which enables efficient carry computation through a tree-structured network with reduced logic depth and balanced fan-out. In the second stage, a BCD correction mechanism is applied; whenever the intermediate sum exceeds 9 or generates a carry, a correction value of 6 is added to ensure a valid BCD output. The overall 32-digit adder is constructed by cascading multiple single-digit BCD adder blocks in a structural manner, allowing carry propagation from the least significant digit to the most significant digit. The complete design is implemented using Verilog HDL with a modular and scalable approach. Functional verification is carried out using a testbench with various input combinations, and performance is evaluated in terms of delay and power consumption. The use of the Brent–Kung architecture significantly improves carry propagation efficiency, resulting in reduced delay and lower power consumption compared to conventional CLA-based designs, making the proposed 32-digit BCD adder suitable for high-performance VLSI applications. The operation of each BCD adder stage in the proposed design consists of the following steps:

1 Digit BCD adder using Brent–Kung Adder

Two 4-bit BCD digits are added using a 4-bit Brent–Kung adder**.** The prefix tree structure computes carry signals in parallel, producing a 4-bit binary sum and a carry output with reduced delay.

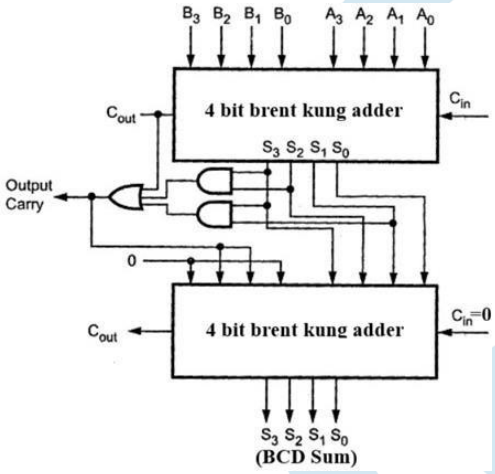

Fig1: 1-digit BCD adder

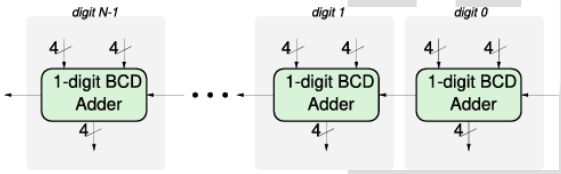

Fig2: N-digit BCD adder

Detection of Invalid BCD Result

The intermediate binary sum obtained from the Brent–Kung adder is checked to determine whether it represents a valid BCD value. The result becomes invalid if:

- The binary sum is greater than 1001 (decimal 9)
- A carry is generated during the binary addition

Brent–Kung Adder Architecture

The Brent–Kung adder is a parallel prefix adder designed to reduce the logic depth required for carry computation. It uses generate (G) and propagate (P) signals to determine carry values efficiently.

The generate and propagate signals are defined as:

1. Pre-possessing stage: Generate and propagate signals to each pair of the inputs A and B are computed in this stage.

- Generate (G) = A · B
- Propagate (P) = A ⊕ B

Using these signals, the carry output for each stage can be computed using prefix operations. The Brent–Kung structure organizes these operations in a tree-like prefix network consisting of multiple levels.

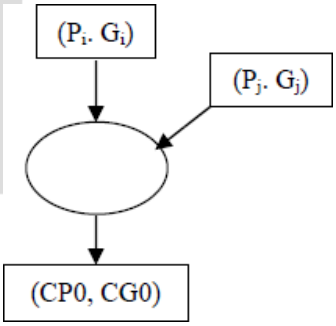

Fig3: Carry network

2. Carry generation network: In this stage, carries equivalent to each bit is calculated. All these operations are implemented and carried out in parallel. Carries in parallel are segmented into smaller pieces after the implementation of the stage. Carry propagate and generate are used as intermediate signals which are given by the logic equations :

CPO = Pi and Pj

CGO = (Pi and Gj) or Gi

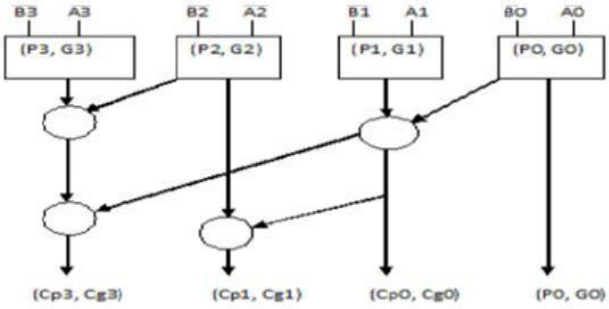

Fig4: carry tree network of brent kung adder

3. Post processing Stage: This is the concluding step to compute the summation of input bits.

$$C_{i-1} = P_i \text{ and } C_{in}$$
$$S_i = P_i \text{ xor } C_{i-1}$$

IV. RESULTS

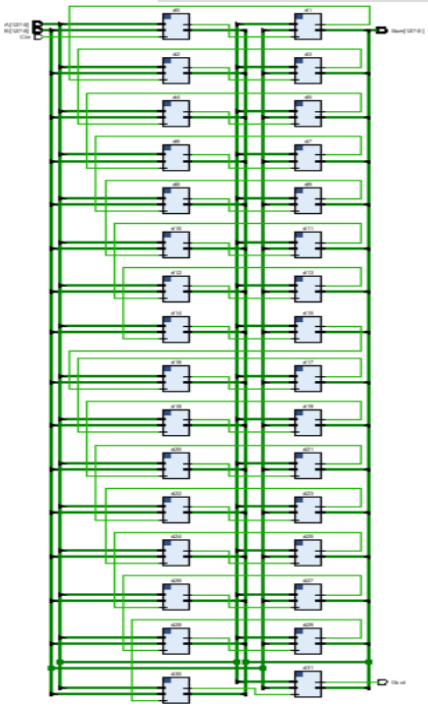

Fig 5: RTL Schematic of 32digit BCD adder using BKA

RTL SCHEMATIC: The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The HDL language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e Verilog, VHDL. The RTL schematic even specifies the internal connection blocks for better analyzing. The figure represented below shows the RTL schematic diagram of the designed architecture.

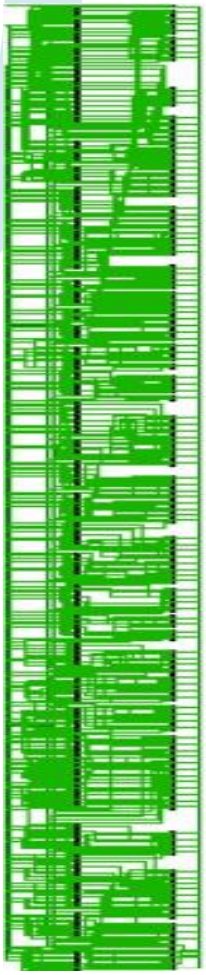

Fig6: Technology schematic of BCD adder using BKA

TECHNOLOGY SCHEMATIC: The technology schematic makes the representation of the architecture in the LUT format, where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design. The LUT is consider as an square unit the memory allocation of the code is represented in there LUT s in FPGA.

SIMULATION: The simulation is the process which is termed as the final verification in respect to its working whereas the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool, and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems.

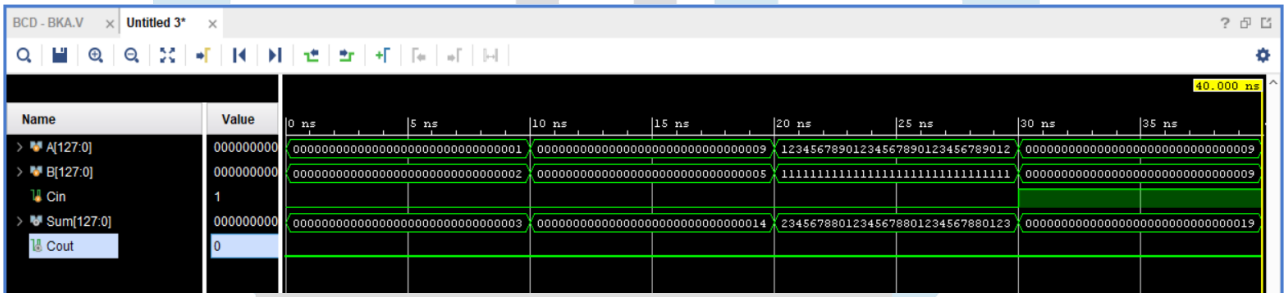

Fig 7: Simulated wave form of BCD adder using BKA

PARAMETERS : Consider in VLSI the parameters treated are area and power ,based on these parameters one can judge the one architecture to other. The table presents a performance comparison between the conventional Carry Lookahead Adder (CLA) based BCD adder and the proposed Brent– Kung Adder (BKA) based BCD adder for a 32-digit configuration. It is observed that the proposed BKA design achieves better performance in both speed and power consumption. The propagation delay is reduced from 2.01 ns to 1.57 ns, resulting in an improvement of approximately 22%. Similarly, power consumption decreases from 123.218 mW to 110.881 mW, achieving around 10% reduction. These results indicate that the BKA-based BCD adder is more efficient than the CLA-based design, particularly for large digit-width operations, due to its optimized carry propagation and reduced logic complexity.

Table 1: Parameter comparison

Parameter	32-digit BCD adder using CLA	32-digit BCD adder using BKA
Speed (ns)	2.01	1.57
Power(mW)	123.218	110.881

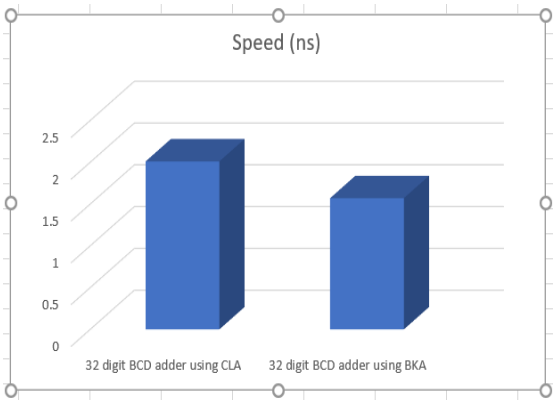

Fig8: speed comparison barograph

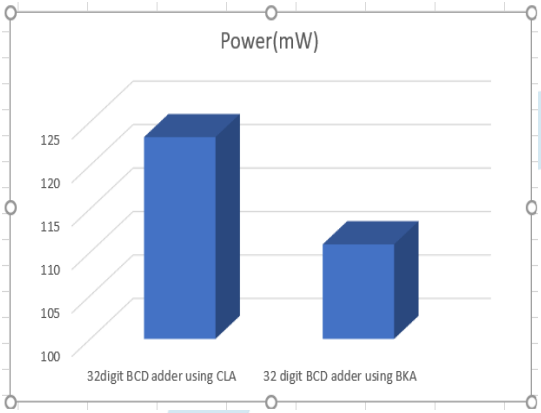

Fig9: power comparison barograph

V. CONCLUSION

This paper presents the design and implementation of multi-digit Binary Coded Decimal (BCD) adders using the Brent–Kung Adder (BKA) architecture and compares their performance with conventional Carry Lookahead Adder (CLA) based designs for both 8-digit and 32-digit configurations. The proposed BKA-based design leverages a parallel prefix structure to achieve efficient carry propagation with reduced logic depth, resulting in improved speed and lower power consumption.For the 8-digit BCD adder, the proposed design achieves a delay reduction of approximately 32% and a power reduction of about 7% compared to the CLA-based design. Similarly, for the 32-digit BCD adder, the delay is reduced by around 22% and power consumption by approximately 10%. These results clearly indicate that the proposed architecture consistently outperforms the existing design across different digit sizes.

Furthermore, the comparison shows that while both designs benefit from the use of parallel carry computation, the Brent–Kung architecture provides better scalability as the number of digits increases. The reduction in delay and power becomes more significant for larger configurations, demonstrating the suitability of the proposed design for high-bit-width decimal arithmetic.

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AUTHORS:

Mrs.K.Rojamani,Assistant Professor in the Department of Electronics and Communication Engineering in Krishna University College of Engg & Tech, Machilipatnam, Andhra Pradesh, India

Email-id: rojamanikru@gmail.com

S.Praneeth Sai, pursuing B.Tech in the Department of Electronics and Communication Engineering in Krishna University College of Engg & Tech, Machilipatnam, AndhraPradesh, India

Email-id: sankarpraneeth668@gmail.com

B.Hanumantha Rao, pursuing B.Tech in the Department of Electronics and Communication Engineering in Krishna University College of Engg & Tech, Machilipatnam, Andhra Pradesh, India

Email-id:
baligodugulahanumantharao@gmail.com

Y.V.V.S.N.Manikanta, pursuing B.Tech in the Department of Electronics and Communication Engineering in Krishna University College of Engg & Tech, Machilipatnam, Andhra Pradesh, India

Email-id: **yenugumanikanta@gmail.com**