Efficient Sequential Circuit Design and Implementation Using 7nm PTM

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***Abstract*—The design and implementation of sequential circuits such as D Flip Flop and Johnson Counter at the 7nm technology node are more challenging due to the strict performance, power, and area constraints inherent in advanced semiconductor scaling. Using an open-source RTL to GDS-II design pipeline and the 7nm Predictive Technology Model (PTM), this work provides a thorough examination of the methods and optimization techniques needed for reliable nanoscale digital systems. The process, which includes high level synthesis, logic optimization, physical design, and verification, shows how notional RTL is converted into silicon layouts that can be manufactured using open-source tools like ASAP7, Yosys, and Open ROAD, as well as predictive process design kits. Targeted solutions are provided for important issues such temporal closure, signal integrity, and leakage power, emphasizing the function of contemporary Electronic Design Automation (EDA) tools in enabling accurate validation and smooth stage integration. Performance measures evaluated experimentally demonstrate how well the 7nm PTM works to create dense, fast, and energy-efficient sequential circuits. For researchers and engineers aiming to create dependable, power-efficient digital circuit designs at the vanguard of semiconductor technology, such findings highlight the vital significance of cooperative, open-source approaches for cutting-edge VLSI innovation.**

***Index Terms*—7nm Predictive Technology Model (PTM), Sequential Circuits, RTL to GDS-II Flow,ASAP7, Yosys, Open-ROAD, FinFET, VLSI Design, Semiconductor Technology Nodes.**

I. INTRODUCTION

A. Background

Continuous advances in semiconductor process technology have enabled the scaling of integrated circuits to the 7nm node and beyond. These advancements introduce significant benefits in device density, speed, and power efficiency, enabled through FinFET devices and current design methodologies [2]. At such advanced nodes, Predictive Technology Models (PTMs) for 7nm play an important role by providing accurate, scalable device and interconnect models that are required for simulation and evaluation of digital circuit concepts [1]. These models serve to bridge the gap between sophisticated fabrication techniques and theoretical design, especially during the simulation and verification stages.

B. Existing Evidence

The ASAP7 Predictive Process Design Kit (PDK) is widely used in academic research to provide scalable 7nm FinFET device and interconnect models with realistic process restrictions, allowing for accurate benchmarking of next generation circuits [3]. Recent research had introduced an optimized ASAP7 predictive technology model and standard cell library, allowing advanced-node digital architectures to be characterized with great fidelity [4]. Open-source digital synthesis has become practical and reproducible thanks to tools like Yosys, which converts high-level RTL specifications into synthesizable netlists. for VLSI flows [5]. Recent studies validate the effectiveness of open-source RTL-to-GDS-II design flows using tools like Yosys for logic synthesis and Open ROAD for physical implementation. These flows allow designers to translate high- level RTL descriptions into manufacturable layouts, facilitating research and education in VLSI design. Tools like Open ROAD further advance the open-source ecosystem by providing an automated RTL-to-GDS-II physical design platform suitable for advanced technology nodes [6]. The development and in- depth characterization of standard cell libraries tailored for 7nm design, particularly using the ASAP7 PDK, have been comprehensively explored in recent literature [7]. The 7nm PTM enables robust simulation of digital circuits to predict their behavior and performance at nanoscale nodes prior A. Specification and RTL Design to committing to physical design. Full RTL-to-GDSII flows using open-source tools at sub-10nm nodes, demonstrating the capability to generate manufacturable layouts for complex circuits, have been successfully reported [8]. Existing evidence demonstrates that a workflow combining predictive simulation models with open-source implementation tools can support realistic power, performance, and area (PPA) analysis for both combinational and sequential circuits. Unique challenges and solutions for designing, modeling, and analyzing sequential circuits like D Flip Flop and Johnson Counter in deeply-scaled FinFET processes, including at sub-10nm nodes, have been systematically addressed in recent work [9].

C. Research Gap

Despite these advances, there is a lack of comprehensive, reproducible studies focusing on sequential circuit design at 7nm, specifically where the PTM is used mainly for simulation and open-source toolchains are used for RTL-to-GDS-II implementation. Prior literature emphasizes either device modeling or combinational logic, without thoroughly investigating unique challenges in sequential system design such as timing convergence, leakage, and noise robustness in deep-nanometer technologies. Few studies systematically document end-to-end open-source flows for the implementation and benchmarking of sequential circuits at this scale.

D. Objective

The objective of this work is to establish a clear, reproducible methodology for the design and implementation of sequential circuits like D Flip Flop and Johnson Counter: employing the 7nm Predictive Technology Model exclusively for simulation and evaluation of digital designs, and utilizing a fully open-source RTL-to-GDS-II flow for actual VLSI implementation, This approach seeks to (i) assess the integration of predictive simulation and physical design using open-source tools, (ii) address key design and optimization challenges for sequential systems at 7nm, and (iii) provide benchmarks and practical guidelines for the VLSI research community.

E. Scope

This research encompasses the full digital design cycle: specification, RTL modeling, simulation with 7nm PTM, open-source synthesis and layout, verification, and PPA evaluation. The study offers approaches and insights geared to both educational and research environments, promoting repeatable innovation for advanced technology nodes through simulation-verified models procedures.

PROPOSED METHOD

The proposed method particulars a reproducible and automated plan for designing and implementing sequential circuits at the 7nm technology node by using the 7nm Predictive Technology Model (PTM) for simulation and open source Electronic Design Automation (EDA) tools for an RTL-to- GDS-II design flow. The procedure, informed by recent IEEE research, consists of the following key steps:

A. Specification and RTL Design

Describe the functional supplies of the target sequential circuit for the D Flip Flop and Johnson Counter. Model the desired hardware performance at the Register Transfer Level (RTL) using hardware description languages such as Verilog or VHDL.

B. Simulation and Evaluation with 7nm PTM

Device-level simulations use the 7nm Predictive Technology Model (PTM) to estimate delay, power, and process changeability before synthesis and layout [1]. Evaluate circuit presentation through simulation before proceeding to physical implementation.

C. Logic Synthesis

RTL design is made using Yosys, an open-source mixture suite proven for modern VLSI logic conversion [5]. Certify the netlist meets timing, area, and power targets suitable for advanced nodes.

D. Automated RTL-to-GDS-II

Physical Design Flow Placement: Assign physical locations to standard cells to minimize congestion and wire length. Routing: Establish all necessary physical interconnections while adhering to design rules and signal integrity constraints. Physical Verification: Conduct Design Rule Checking (DRC) and Layout Versus Schematic (LVS) to ensure all physical and logical constraints are satisfied. Static Timing Analysis (STA): Perform static timing analysis on the post-routed design to verify that all timing constraints are met and to identify any timing violations before tape-out. Finally, difficult static timing analysis ensures all sequential and timing limitations are met, justifying challenges unique to sub-10nm sequential circuit like D Flip Flop and Johnson Counter operation [9]. GDS-II Generation: Generate the final GDS-II layout for fabrication. This end-to-end workflow leverages the predictive modeling capabilities of the 7nm PTM for accurate simulation, and the automation of modern open-source RTL-to-GDS-II design flows—making advanced, nanoscale VLSI design both accessible and reproducible for academic and industrial researchers.

II. METHODOLOGY

A.D Flip Flop

Schematic Design (Cadence Virtuoso with 7nm PTM)

A D flip-flop from Fig 1 and Fig 2 was designed at the transistor level in Cadence Virtuoso, using MOSFET parameters from the 7nm PTM for realistic device modeling. The schematic included key features such as setup/hold paths and clocked operation. Pre-layout simulations were performed using the Spectre simulator to validate functional correctness and extract timing metrics (e.g., clock-to-Q delay, setup, and hold times). Power consumption and switching characteristics were also measured to guide further optimization.

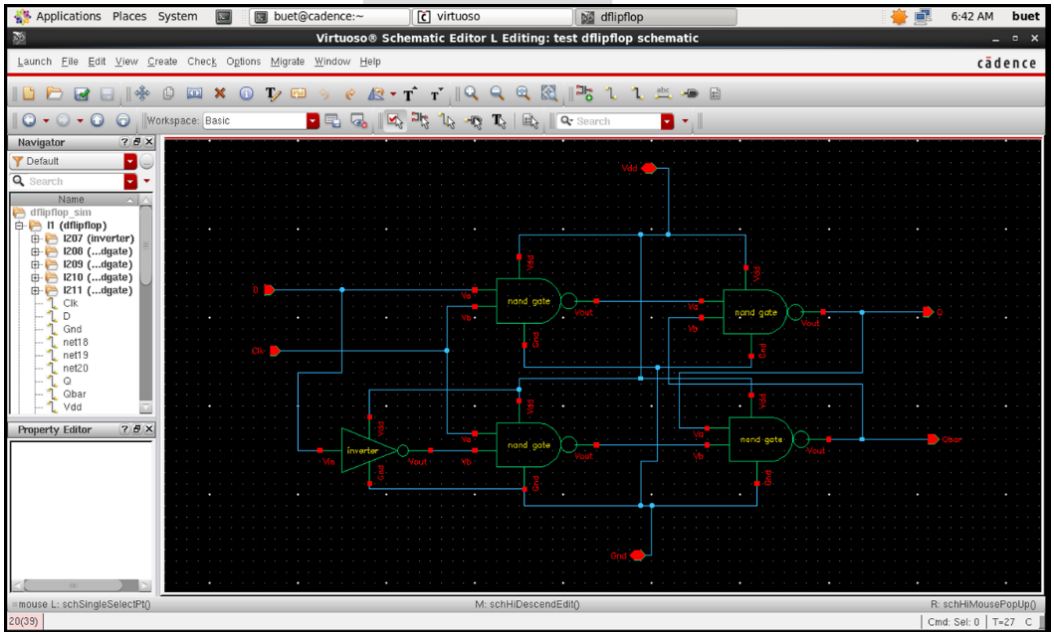

Fig. 1. Schematic of D Flip Flop

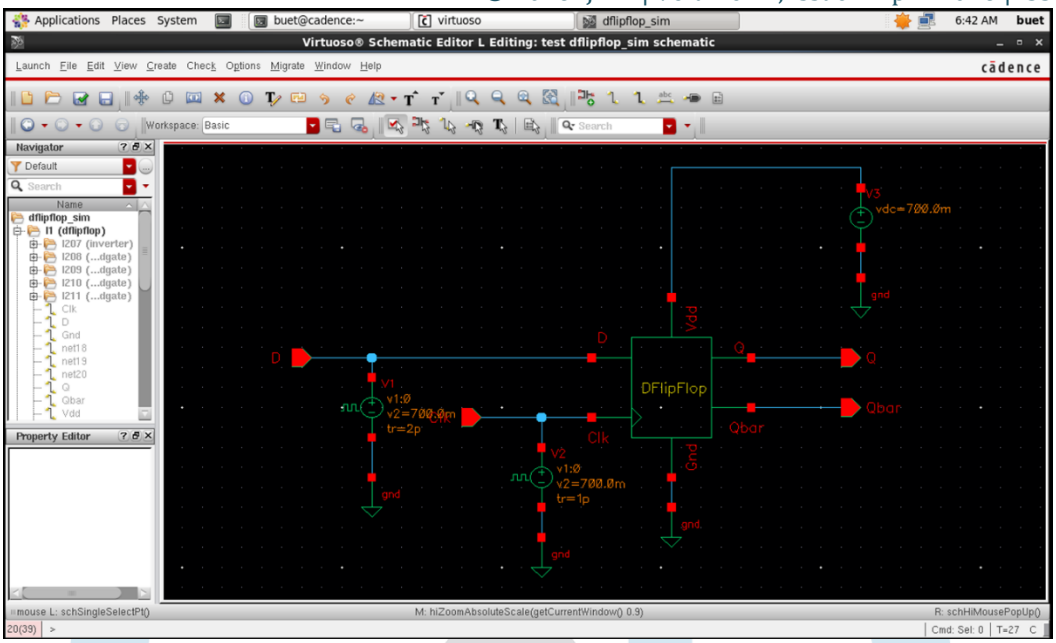

Fig. 2. Symbol of D Flip Flop

RTL-to-GDS-II Implementation (Qflow)

The D flip-flop function was described in Verilog for RTL synthesis and simulation. Using Qflow, RTL was synthesized to a gate-level netlist with Yosys. Automated placement and routing was performed with GrayWolf and Qrouter, resulting in a physical layout. Static timing analysis (STA) was used to verify compliance with timing constraints Design Rule Checking (DRC) and Layout Versus Schematic (LVS) checks were run to ensure correctness. Post-layout.

B. Johnson Counter

Schematic Design (Cadence Virtuoso with 7nm PTM)

The Johnson counter from Fig 3 and Fig 4 implemented as sequential ring counter with feedback, using suitable chain of D flip-flops in Cadence Virtuoso and 7nm PTM models. Transistor-level schematics were simulated with custom stimulus to validate serial shift, feedback operation, correct output sequences. Key performance metrics such as frequency, power, functional robustness across process variation were extracted.

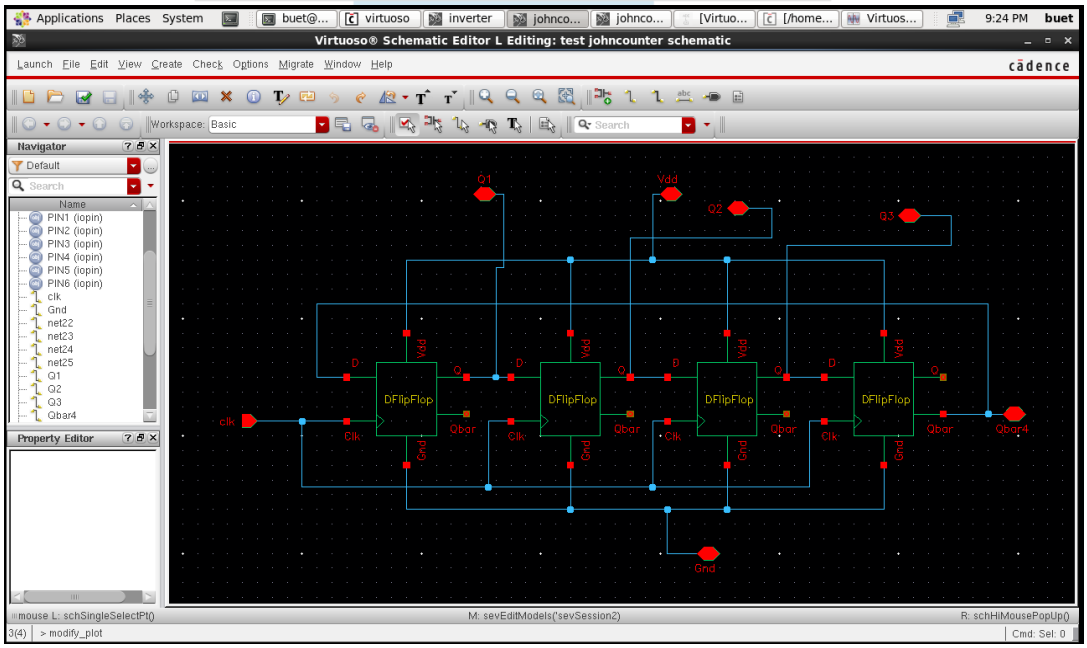

Fig. 3. Schematic of Johnson Counter

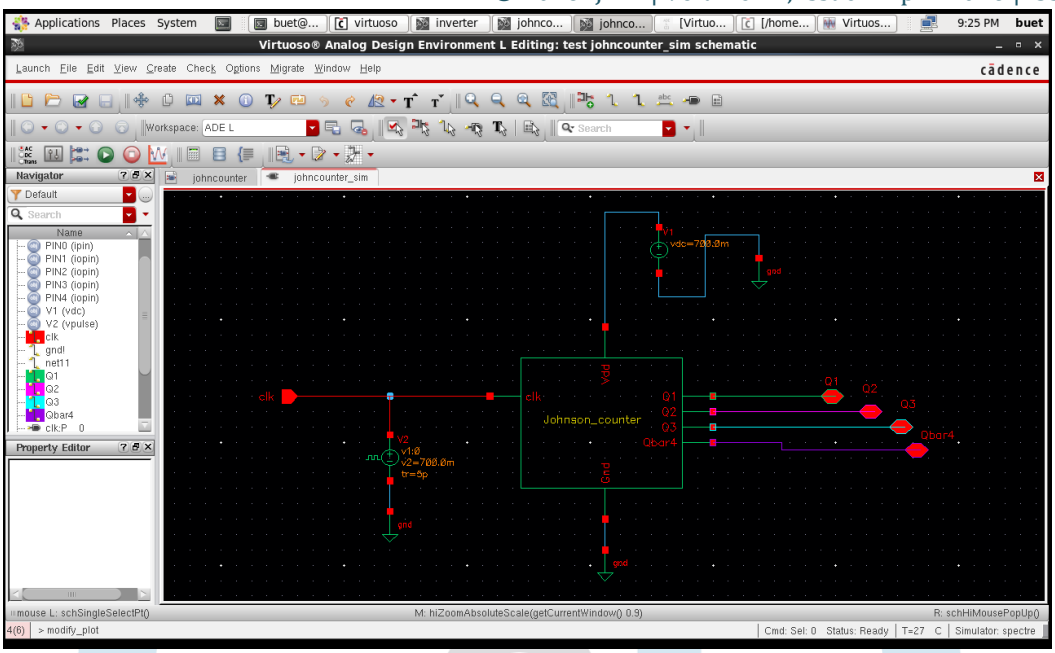

Fig. 4. Symbol of Johnson Counter

RTL-to-GDS-II Implementation (Qflow)

The Johnson counter was modeled in Verilog at RTL, parameterized for N stages as needed. Synthesis was performed with Yosys via the Qflow tool, targeting a standard cell library for placement and routing by GrayWolf and Qrouter. STA ensured the counter met clocking and data propagation require- ments at nanoscale speeds. DRC and LVS validated the post- layout design before GDS-II export. The generated GDS-II file and post-layout simulations confirmed accurate operation, logic sequence, and performance as intended.

III. SIMULATIONS AND RESULTS

A. D Flip Flop

Simulation in Cadence Virtuoso with 7nm PTM

Run transient (time-domain) simulations from Fig 5 using Spectre, capturing waveforms for D, CLK, and Q. Measure performance metrics such as clock-to-Q delay, setup and hold times, and switching power consumption. Analyze the output Q waveform to verify correct flip-flop operation under different input timing scenarios and extract timing margins and energy per transition.

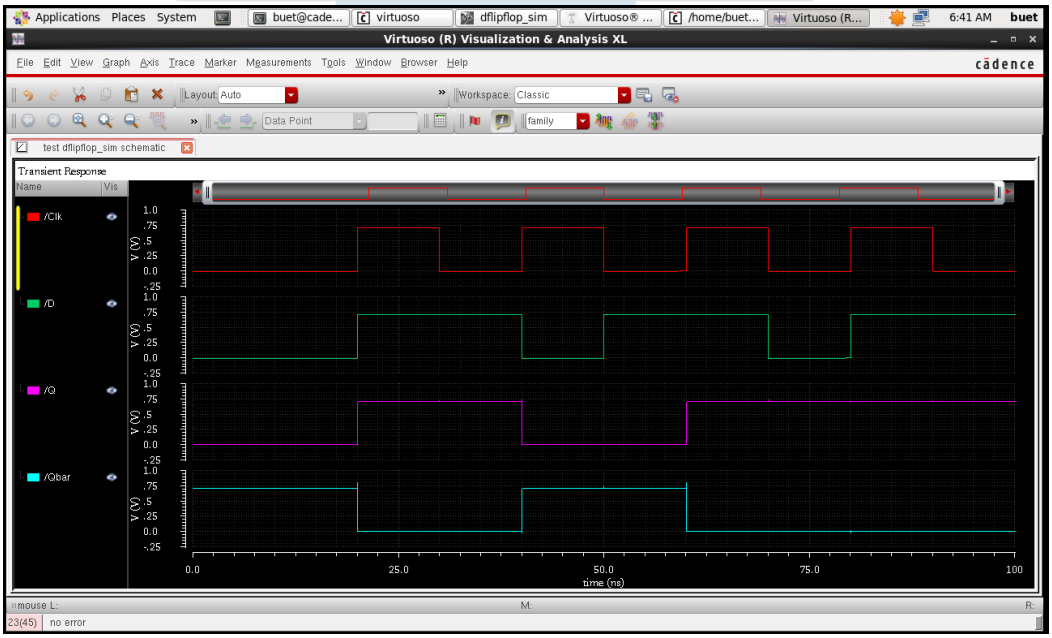

Fig. 5. Transient Response of D Flip Flop

RTL-to-GDS-II Implementation with Qflow

Use Yosys (invoked by Qflow) to synthesize the RTL to a gate-level netlist, mapping logic to standard cells. Run Gray- Wolf and Qrouter (via Qflow) for automated cell placement and routing, producing a physical layout from Fig 6.Confirm that the post-routed design meets timing constraints using Qflow's built-in STA tools. Ensure correctness through automatic DRC/LVS, then export the final GDS-II from Fig 7 file for tapeout or further analysis.

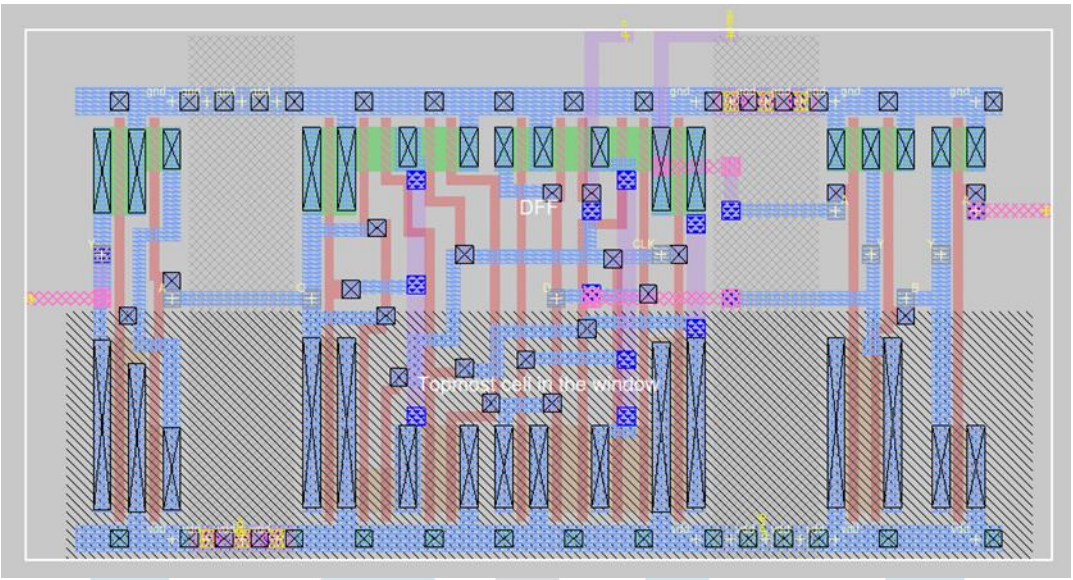

Fig. 6. Layout of D Flip Flop

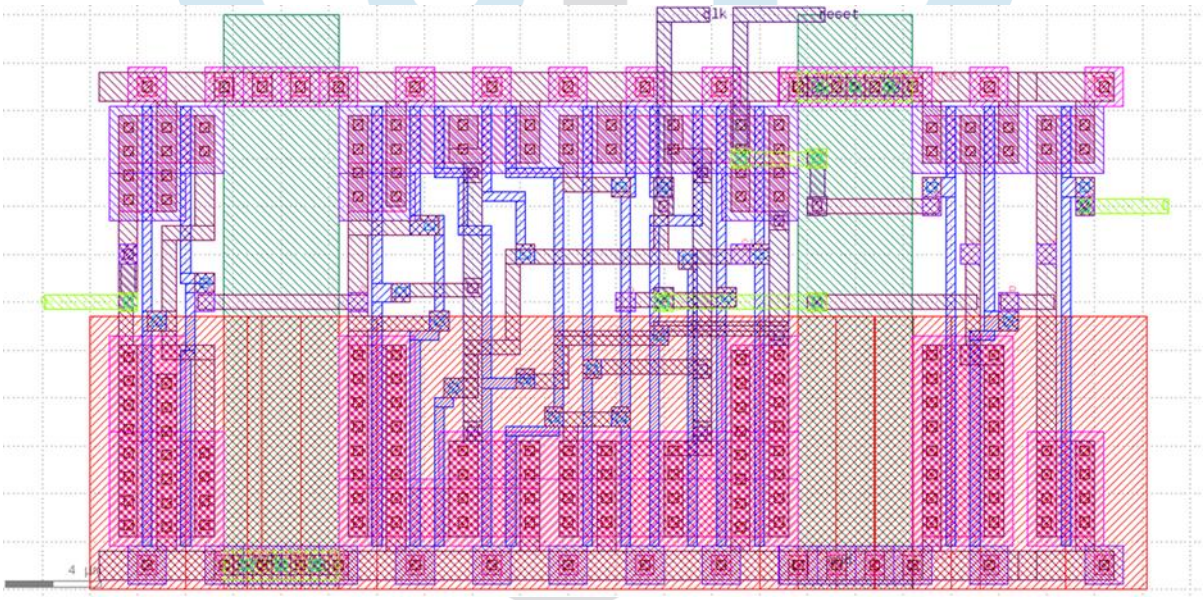

Fig. 7. GDS-II of D Flip Flop

B. Johnson Counter

Simulation in Cadence Virtuoso with 7nm PTM

Simulate multiple clock cycles from Fig 8 and capture Q outputs of all flip-flops involved. Verify the correct state sequence, roll-over behavior, measure propagation delays for each stage, and analyze power consumption for a complete count cycle.

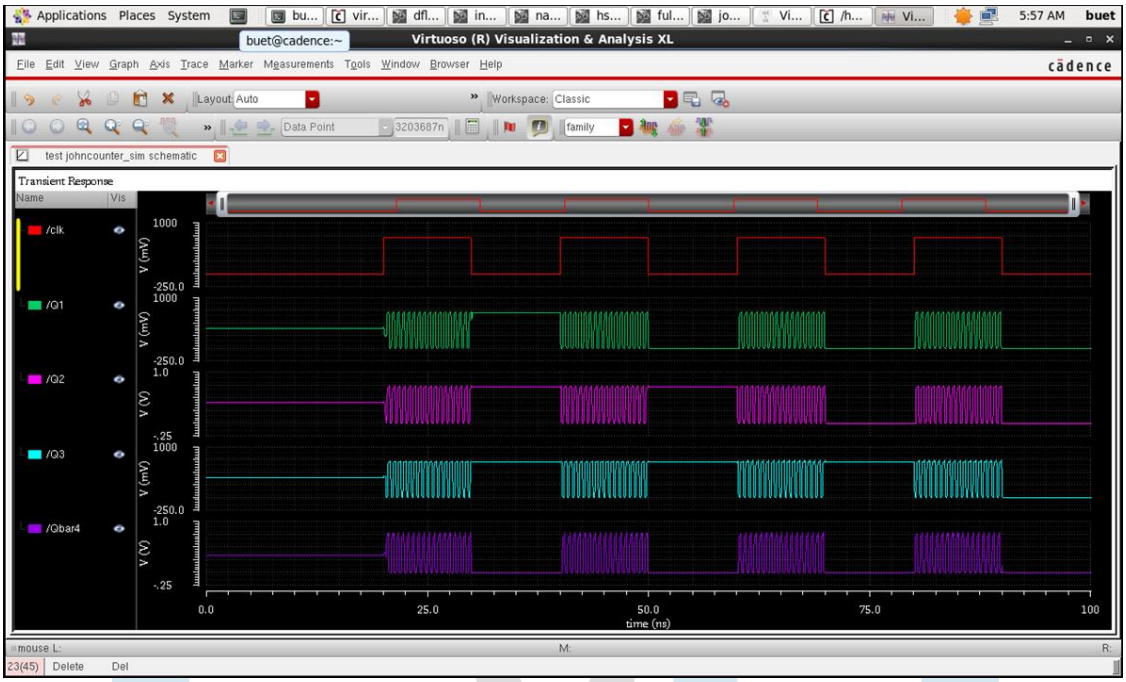

Fig. 8. Transient Response of Johnson Counter

RTL-to-GDS-II Implementation with Qflow

Use Yosys through Qflow to generate an optimized gate- level netlist. Employ to complete cell placement and routing and to produce layout from Fig 9 by using Q Flow automation . Ensure all flip-flop stages meet timing requirements using STA within Qflow. Run DRC/LVS to validate physical correctness and export the final GDS-II file from Fig 10.

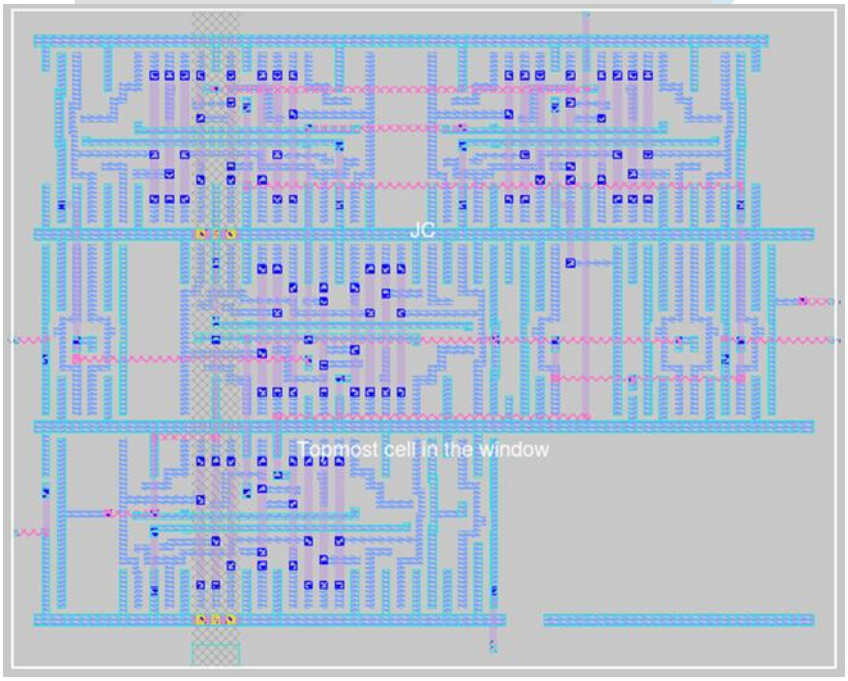

Fig. 9. Layout of Johnson Counter

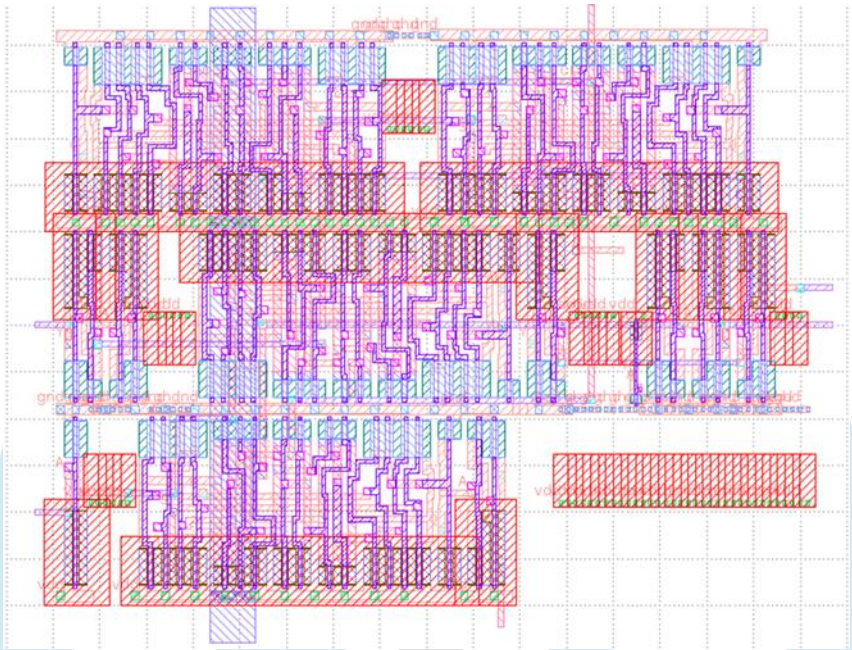

Fig. 10. GDS-II of Johnson Counte

Metric	Reference D Flip-Flop [1]	Proposed D Flip-Flop
Technology Node (nm)	45	7
Supply Voltage (V)	1.0	0.7
Area (μm^2)	5.11	0.124
Delay (ps)	90	3
Power (µW)	104	5.5
Rise Time (ps)	50	2.56
Fall Time (ps)	45	2.90

TABLE I SIMULATION ANALYSIS OF 7NM PTM VS. 45NM REFERENCE D FLIP-FLOP

Simulation results from TABLE I indicate a significant reduction in propagation delay as technology is scaled from 45nm to 7nm. For both the D flip-flop and Johnson counter, the average clock-to-Q (D flip-flop) and stage propagation delays (Johnson counter) dropped due to shorter channel lengths and improved carrier mobility at the 7nm node. However, process variation and increased short-channel effects slightly limit the ideal improvement at the smallest nodes. Total dynamic and leakage power measurements show that circuits implemented with the 7nm PTM consume dramatically less dynamic power than those at 45nm, attributed to lower supply voltage and gate capacitances. However, leakage power becomes a larger fraction of the total at 7nm due to increased subthreshold leakage. Both rise and fall times of output waveforms improved due to faster switching capabilities and reduced parasitic loads in 7nm transistors. This results in steeper output transitions, which benefit high-frequency operation but may present new challenges for signal integrity. Physical layout area for both circuits was substantially reduced at 7nm. Standard cell height, routing track pitch, and minimum feature size are all much smaller, allowing denser packing and reduced die size per function. The use of open-source digital flows still presents some area overhead compared to hand tuned commercial flows, but the relative gain from scaling is robust.

IV. CONCLUSION

This work demonstrated a wide-ranging methodology for the design and operation of sequential circuits specifically, a D flip-flop and a Johnson counter leveraging the 7nm Predictive Technology Model (PTM) for accurate simulation and open-source automation (Q flow) for well-organized RTL-to-GDS-II realization. Our proportional analysis between 45nm and 7nm PTM revealed marked improvements at the advanced node, including considerable reductions in propagation delay, dynamic power consumption, rise/fall times, and physical area. While leakage power becomes more distinct at 7nm, the gains in performance and density highlight the efficiency of constant technology scaling.

V. ACKNOWLEDGMENT

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