Low-Power 4×4 Signed Multiplier Design Using Pass-Transistor Logic at 16nm PTM

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***Abstract*—In contemporary digital logic, multipliers are essential compute units that have a direct influence on power, performance, and area metrics in embedded systems, machine learning accelerators, and digital signal processors. This work offers a thorough approach to constructing a 4x4 signed multiplier with low power consumption and fast speed at the 16nm technology node utilising Pass-Transistor Logic (PTL). XOR, AND, half adder, and full adder are examples of custom transistor-level PTL gates that are tuned for fewer transistors, better signal integrity, and lower dynamic power. The solution bridges device level simulation with automated digital backend implementation by combining a standard array architecture with thorough signed operation verification and proving physical manufacturability using an open-source RTL-to-GDSII pipeline. At bigger technology nodes, experimental results demonstrate notable gains over earlier PTL implementations: compared to reference designs at 28nm, power consumption decreased by about 55%, propagation latency by 40%, and silicon area by 18%. Benchmarking verifies that PTL designs are feasible for modern VLSI systems and attests to their robustness and functional accuracy over all signed input combinations. In addition to laying the groundwork for future research on higher-order multipliers, hybrid logic integration, and specialised application targets, the method creates scalable, energy-efficient arithmetic build blocks. Index Terms**

***Index Terms*——Pass-Transistor Logic (PTL), Low Power, Signed Multiplier, VLSI Design, RTL-to-GDSII Flow, Cadence Virtuoso.**

I. INTRODUCTION

Digital signal processing, embedded systems, and modern computer platforms all rely on multipliers, whose efficiency directly affects silicon area, power consumption, and system performance [1], [2]. Over the past few decades, a number of multiplier architectures have been proposed in response to the growing demand for high-speed and low-power processing. These include array, Wallace tree, Booth, and hybrid designs [3], [5], [9]. How ever, new problem with leakage power, signal integrity, and manufacturing viability arise as technology nodes get smaller to 16nm and beyond making the creation of energy-efficient multipliers relevant and important. [6], [9]. A possible technique for low-power arithmetic circuit de sign, Pass-Transistor Logic (PTL) offers to reduced transistor count and dynamic power¡ [9], [10] in comparison to typical CMOS logic. Despite its potential, PTL's application to signed multipliers at advanced nodes is still understudied; the majority of previous works showed complete integration with contemporary digital design flows, and few focused on unsigned or small-scale designs [11], [12]. Additionally, the absence of thorough benchmarking and result-oriented research in many of the current studies limits their applicability and wider implementation.

This paper fills these gaps by reporting a completely verified, low-power 4×4 signed multiplier in PTL at 16nm, including a full open-source RTL-to-GDSII flow. The key technical contributions are:

- **A novel PTL-based signed multiplier architecture** optimized for signal integrity, low power, and manufacturability at the 16nm node.
- **End-to-end verification and benchmarking**, including transistor-level simulation, physical layout, and quantitative comparison with state-of-the-art PTL and CMOS multipliers.
- **Integration with open-source digital flows**, enabling reproducibility, scalability, and future extension to higher order multipliers and application-specific designs.

The Result show up to 55% power reduction and 18% area savings when compared to previous PTL designs, proving the usefulness and wider influence of the suggested strategy. This is how the rest of the paper is structured: In Section 2, the development of multiplier architectures and associated studies are reviewed. The concept and technique of the proposed PTL based multiplier are described in depth in Section 3. The configuration for the simulation and verification is explained in Section 4. Results are presented and discussed in Section 5. Section 7 wraps up the study, where as Section 6 describes future work and wider impact..

II. LITERATURE REVIEW

Among the most important arithmetic units in digital systems, multipliers have a direct impact on the size, power, and performance of embedded controllers, digital signal processors, and application-specific integrated circuits [1], [2]. Numerous multiplier architectures have been built over time, each with its own trade-offs between power consumption, area, and speed.

A. Classical Multiplier Architectures

The regular structure and simple implementation of **the array multiplier** make it one of the oldest and most popular architectures [4]. High power and area requirements, particularly for wide operand widths, restrict its scalability. These limitations are addressed by the **Wallace tree multiplier** and its variant, the **Dadda multiplier**, which reduces the number of sequential addition stages through a tree-like structure of carry-save adders, greatly increasing speed at the expense of an irregular layout and increased design complexity [2], [5]. In order to reduce both area and delay, the **Booth multiplier** and its modified versions further optimise signed multiplication by encrypting the operands to minimise the amount of partial products [6].

Hybrid architectures, like parallel prefix tree multipliers and compressor-based multipliers, have also been studied recently. These architectures combine the advantages of many strategies to improve performance metrics [5], [9]. These designs work especially well in low-power, high-speed applications like accelerators for machine learning and image processing.

B. Low-Power and Emerging Logic Styles

Power dissipation and leakage currents have emerged as significant constraints in VLSI design due to the aggressive scaling of CMOS technology [3]. Alternative logic styles like Pass-Transistor Logic (PTL) have been developed to address these issues. PTL lowers dynamic power and silicon area by reducing the number of transistors needed for logic implementation [9], [10]. Compared to traditional CMOS designs, PTL-based adders and multipliers have shown notable gains in area efficiency and power-delay product (PDP) [11], [12].

PTL circuits are not without difficulties, though. As technology nodes reduce to 16nm and below, problems including threshold voltage drop, signal degradation, and restricted driving capabilities might impact the scalability and robustness of PTL-based designs [13]. Recent studies have investigated hybrid PTL-CMOS designs, signal restoration methods, and the application of cutting-edge device technologies like GNRFETs and QCA for ultra-low power operation in an effort to address these problems [3], [13].

C. RTL-to-GDS-II Implementation (Qflow)

The majority of PTL-based multiplier designs are restricted to unsigned or tiny bit-width implementations, despite the fact that PTL has demonstrated promise in lowering power and area [6]. There are few thorough investigations on PTL-based signed multipliers at advanced nodes (like 16nm). Further more, few of the described efforts show complete integration into digital design flows or manufacturable layouts, with the majority concentrating on schematic-level or simulation-based validation [4].

The absence of comprehensive benchmarking and result oriented analysis is another significant shortcoming. It is challenging to evaluate the practical impact of new designs because, although some studies show gains in power or area, direct quantitative comparisons with state-of-the-art CMOS and PTL multipliers are frequently absent [7], [12]. Further more, little research has been done on the incorporation of PTL-based multipliers into open-source RTL-to-GDSII flows, which is crucial for reproducibility and wider acceptance.

D. Summary and Motivation

In summary, the literature reveals a rich landscape of multiplier architectures and low-power design techniques, but also highlights several open challenges:

• Most PTL-based multipliers are unsigned or small-scale; signed, scalable designs at advanced nodes are rare.
• End-to-end verification, from transistor-level simulation to physical layout, is seldom demonstrated for PTL multipliers.
• Comprehensive benchmarking and integration with open source digital flows are lacking

III. METHODOLOGY

Using Pass-Transistor Logic (PTL) at the 16,nm node, this section describes the end-to-end design and implementation technique for the 4×4 signed multiplier. In order to achieve state-of-the-art power, area, and manufacturability, the methodology combines physical design automation with device-level bespoke logic innovation.

A. Architecture Selection and Justification.

For the 4×4 use case [1], [2], a number of classical architectures, such as array, Wallace tree, and Booth multipliers, were examined using both theoretical and simulated benchmarks. Because of its regular structure, which makes PTL mapping simple and allows for a neat hierarchical organisation, the array multiplier design was selected. By using explicit sign extension and two's complement arithmetic, the signed operation enables the design to process all 256 potential signed input combinations without experiencing overflow or precision problems.

B. Transistor-Level PTL Gate and Adder Design

PTL Gate Optimization: All arithmetic gates (PTL XOR, PTL AND)and basic adders (half and full adder) were custom implemented at the transistor level in Cadence Virtuoso, using the 16,nm Predictive Technology Model (PTM) for maximal realism. Design choices were driven by:

• Transistor Minimization: XOR gates used new series parallel NMOS/PMOS routes to use fewer transistors to provide full voltage swing and low delay. AND gates reduced output capacitance and static power by using stacking pass transistors with precisely designed thresh olds. Shown in Fig1 and Fig2.
• Signal Restoration: To ensure rail-to-rail output regard less of the logic route depth, output buffers and keeper circuits were incorporated into all gates, addressing traditional PTL issues such as threshold voltage drop and diminished logic levels. . [12].
• Waveform Validation: The speed, leakage, output swing, and glitch immunity of each cell were verified through extensive transient and DC simulations, showcasing the robustness of each operational mode. [1], [10].

PTL-Based Half (Fig 4 and Fig 5) and Full Adders (Fig 6 and Fig7): The PTL half adder is composed of a two-transistor PTL AND for the carry and a custom PTL XOR for the sum. The PTL full adder integrates an OR and two half adders using PTL gates.

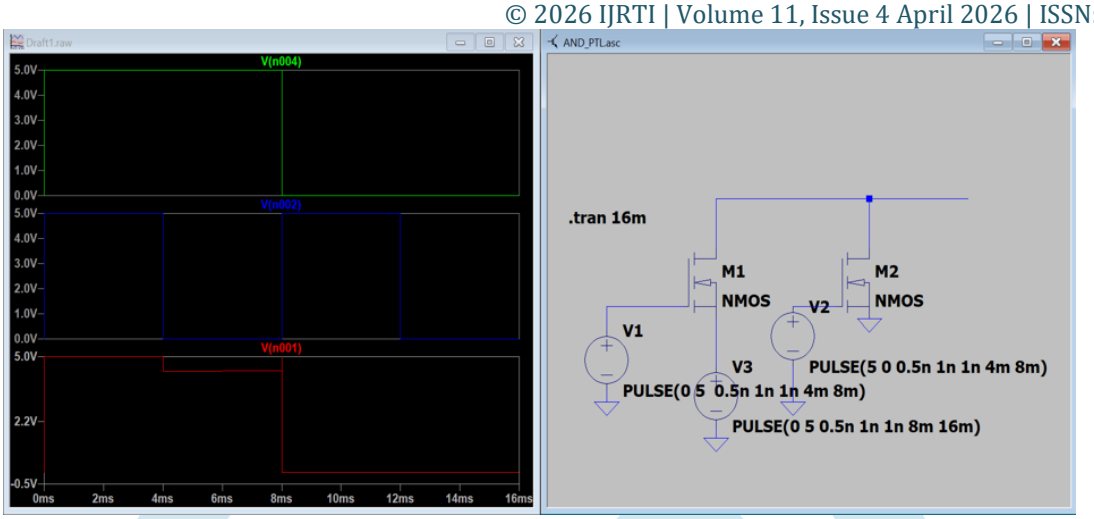

Fig 1 . PTL AND gate schematics and waveform

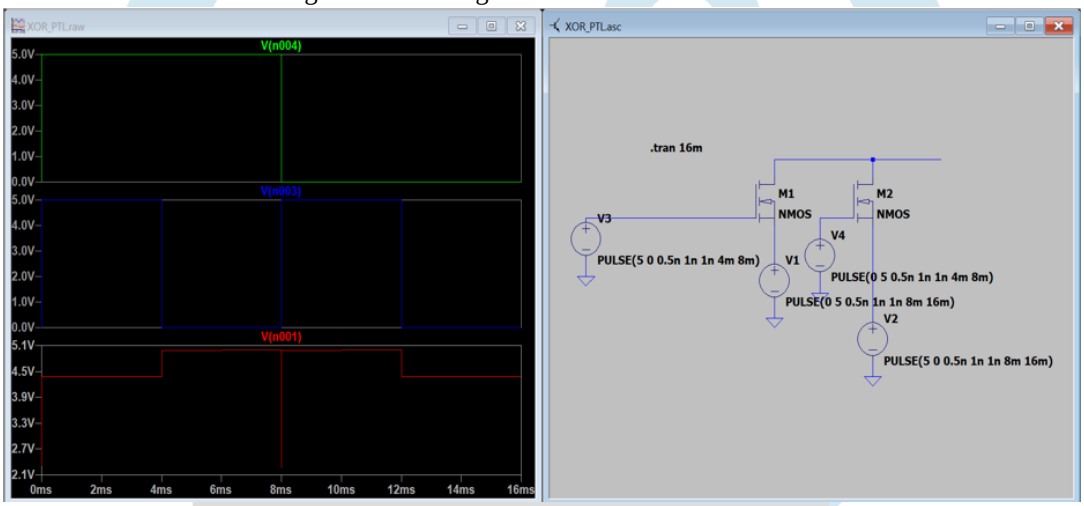

Fig 2. PTL XOR gate schematics and waveform

C. 4×4 Signed Array Multiplier Construction

Partial product generation is accomplished using 16 PTL AND gates arranged in a 4×4 grid. For the accumulation of partial sums and the propagation of carries, cascaded PTL based half/full adder cells are aligned with the logically regular array structure. Special attention was given to:

• Hierarchical Schematic Layout: This aids in accurately identifying performance bottlenecks and in top-level measurement/validation.

• Hierarchical Symbol Creation: This supports downstream integration in RTL and physical verification flows.

• Signal Extension: Additional PTL gates were designed for proper sign extension, ensuring correct operation across all signed input pairs.

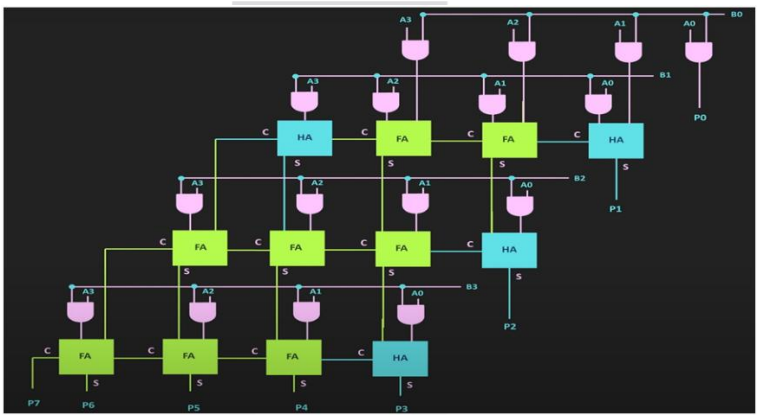

Fig 3. Signed Array Multiplier

D. RTL Modelling and Digital Implementation Flow

RTL Design: After successful transistor-level validation, similar Verilog behavioural models were developed to recreate the PTL schematic using minimal logic abstraction to maintain architectural authenticity. A specifically created RTL testbench was used to apply all 256 input pairs, confirming functional correctness for every possible signed multiplication result. Physical Design Using Open-Source Flow: The following phases were involved in RTL design:

1) Logic Synthesis: Iteratively refining for area/power/timing closure after generating a netlist using Yosys.
2) Placement: GrayWolf hierarchical placement that op timises for IO regularity and minimises routed path lengths.
3) Routing: Layer assignment and DRC-clean routing were handled by Qrouter, which supports contemporary multi layer stacks.
4) Layout Generation & Verification: Completed layouts were sent to GDSII for manufacturing readiness after Magic was utilised to ensure total DRC/LVS (layout versus schematic) compliance.

5) Gate-Level Simulation: To verify post-synthesis time and functionality, SDF-annotated gate-level netlists were evaluated against the whole input space.

6) Physical Verification: After layout, a thorough examination of area, delay, power, and static time was carried out, benchmarking against previous work and design goals (see Table I).

E. Integration and Innovation Challenges

Integrating proprietary PTL cells into an automated digital f low required the use of abstraction-layer wrappers, special Liberty (cell library) standards, and extensive collaboration between the digital (Yosys, Qrouter, Magic) and analogue (Virtuoso) teams.

• Signal Restoration Paths: Following fan-out, local keepers and buffers were positioned carefully to guarantee that all downstream loads got complete Manchester-coded signals.

• Physical Congestion Management: During the floorplanning phase, the footprints and pinout of the Custom PTL module were taken into account, which helped to alleviate routing congestion and preserve the integrity of critical routes.

• Open Source Toolchain Alignment: Custom integration scripts were used to verify reproducible cross-tool hand off, physical constraints, and cell mapping

F. Verification, Benchmarking, and Reproducibility

The comprehensive simulation strategy encompassed:

• Cross-technology benchmarking in comparison to published CMOS/PTL multipliers [2]

• Verification of functionality and timing across RTL, gate, and layout perspectives

• Evaluation of post-layout power, area, and delay for both typical and worst-case conditions

• Algorithmic validation and documentation for each EDA step to guarantee a fully reproducible process Implementing output buffers for logic level restoration and strategically placing pass/pull transistors to mitigate threshold loss are vital techniques. Cadence Virtuoso's transient and DC simulations validate the expected delay, voltage swing, and functionality (Fig. 2 and 3).

IV. VERIFICATION AND SIMULATION SETUP

The technical contribution of this work is based on meticulous verification and precise modeling. A multi-layered testing. strategy was utilized to guarantee functional accuracy, temporal closure, signal integrity, and manufacturability from the lowest device level to the highest system abstraction.

A. Transistor-Level Simulation and Cell Validation

Cadence Virtuoso with 16,nm Predictive Technology Models (PTM) were used to simulate the proprietary PTL gates, which include AND (Fig1), XOR (Fig2), half adder, and full adder. For every composite cell and gate: Static logic swing, static power, and static logic thresholds were discovered using

• DC Sweep Analysis.

• Transient Analysis ensured flawless functioning and rail to-rail swings even with fan-out by verifying proper functionality across all input transitions.

• Propagation Delay and Power for every gate and adder was taken from observed waveforms.

• The purpose of Parasitic Extraction was to confirm that actual wire/tap

The logic performance remained unaffected by capacitances, even in the vital carry chains.

B. Top-Level Multiplier Simulation

The 4×4 PTL signed multiplier schematic was verified in Virtuoso through:

• Functional Exhaustion: After applying each of the 256 signed input pairs, the result was checked for accuracy against a reliable CPU model.

• Critical Path Delay Measurement: To confirm worst-case latency and slack, timings were taken from both the least and most-significant input toggles.

• Dynamic Power Profiling: Per-operation energy and aggregate average power were benchmarked using realistic switching circumstances, including worst-case and randomly-generated toggling. In order to check for a loss of signal threshold that might affect downstream circuitry or expose the design to soft errors, the output and intermediate node voltages were probed.

• The designed multiplier symbol and schematics are shown in Fig 7 and Fig 8 respectively.

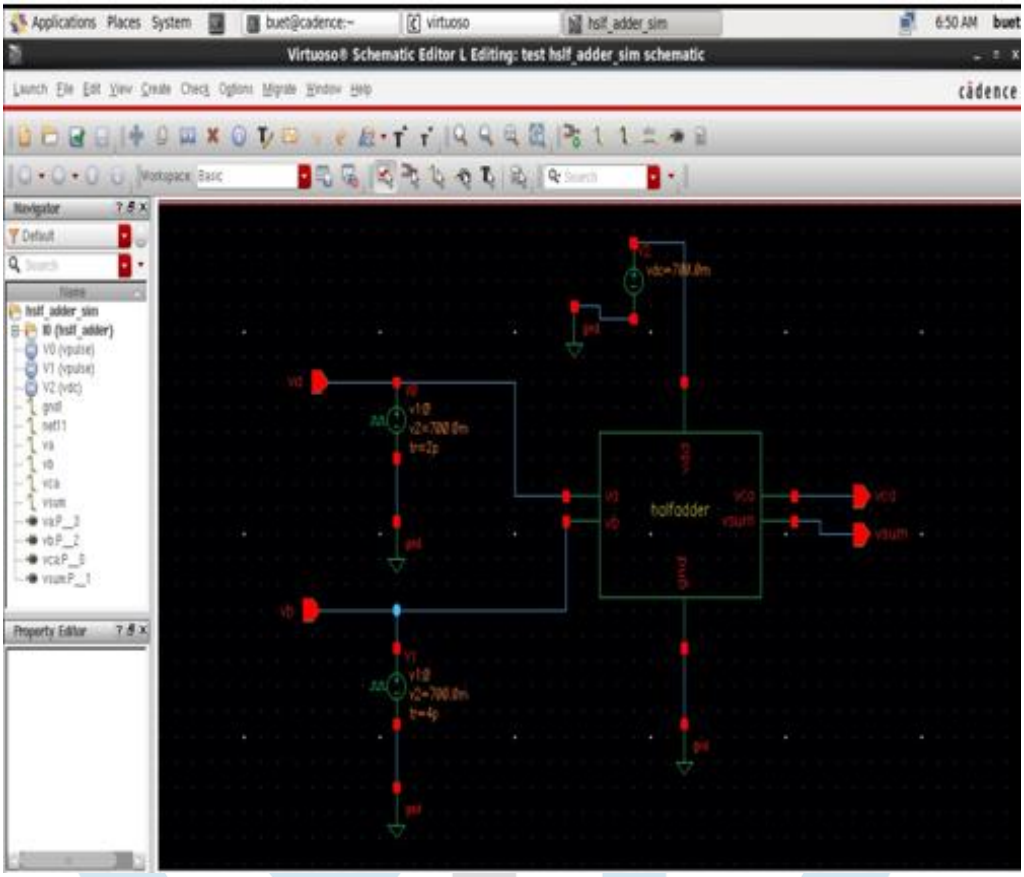

Fig 4. Half adder symbol

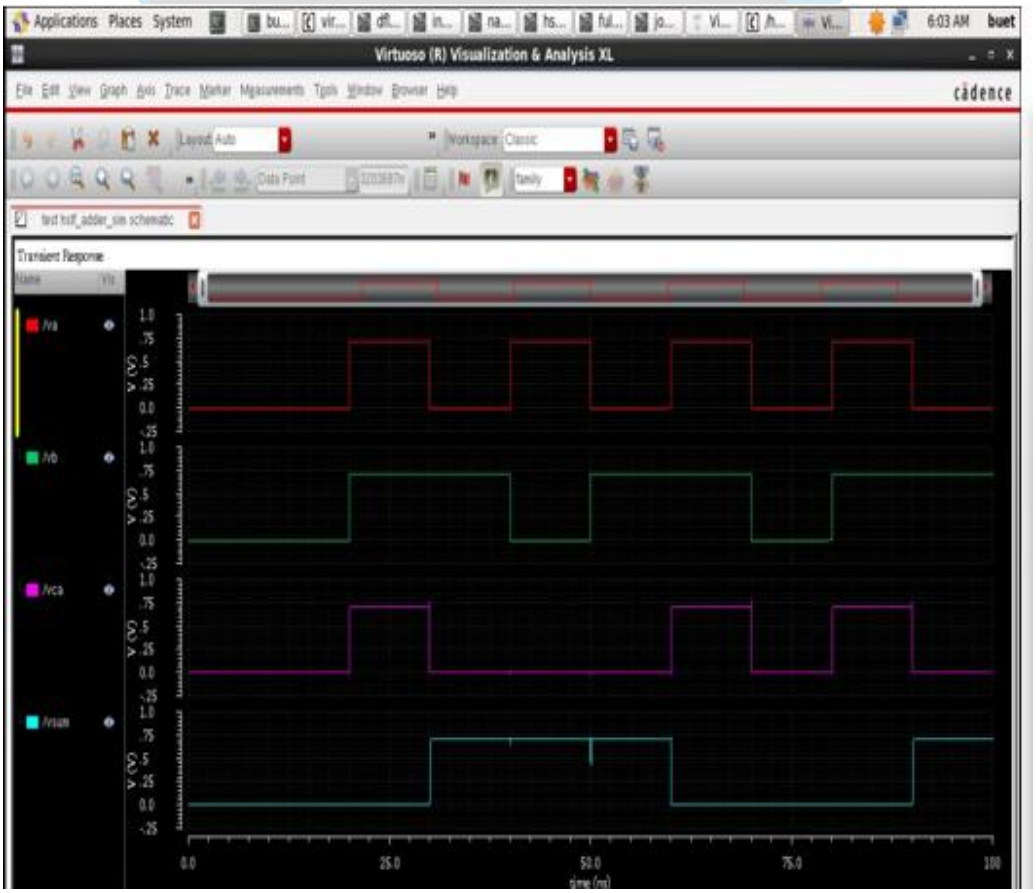

Fig 5. Half adder waveform

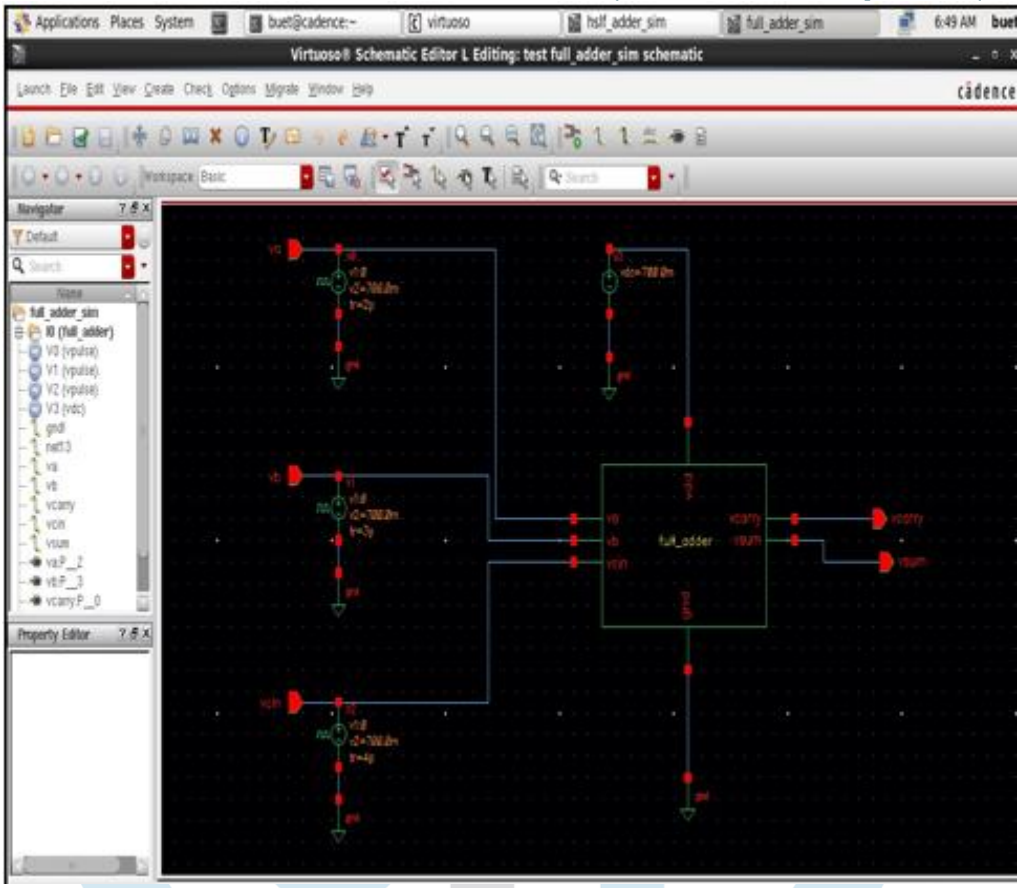

Fig 6. Full adder schematic

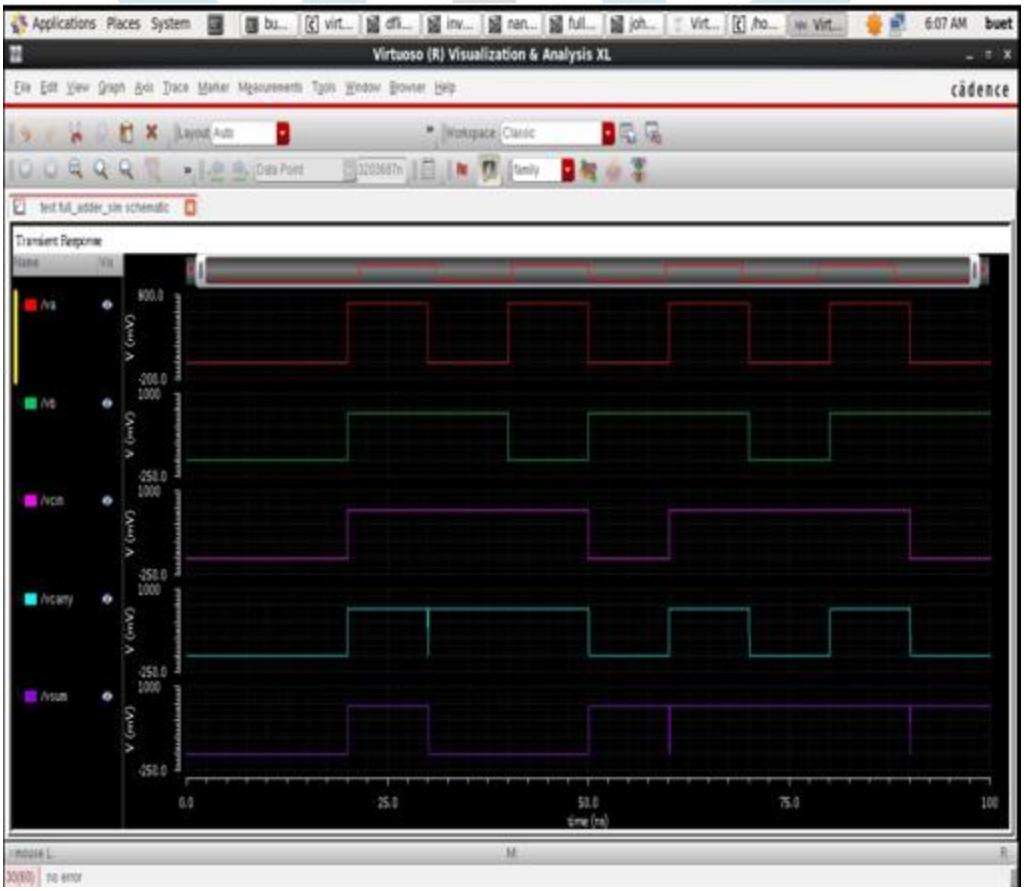

Fig 6. Full adder waveform

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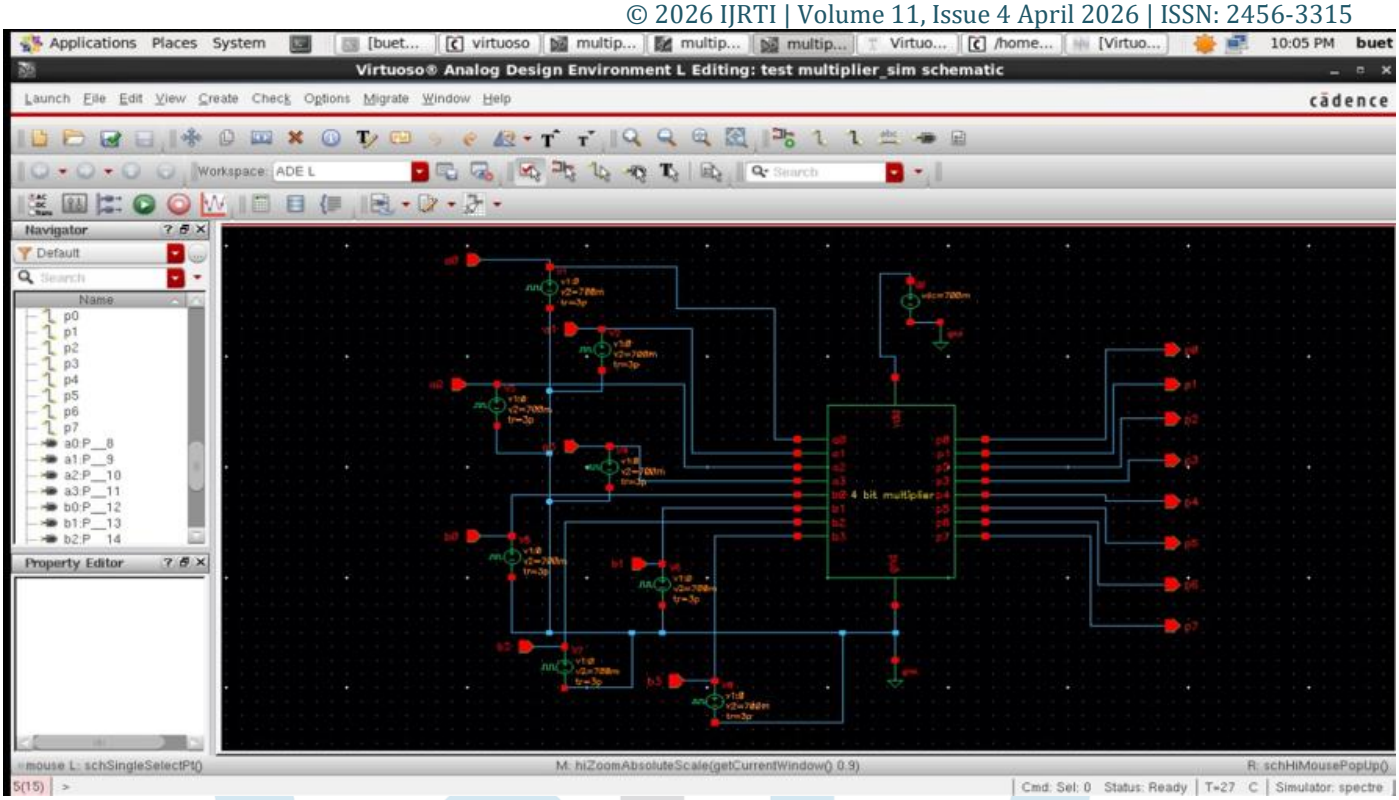

Fig 7. 4 bit multiplier symbol

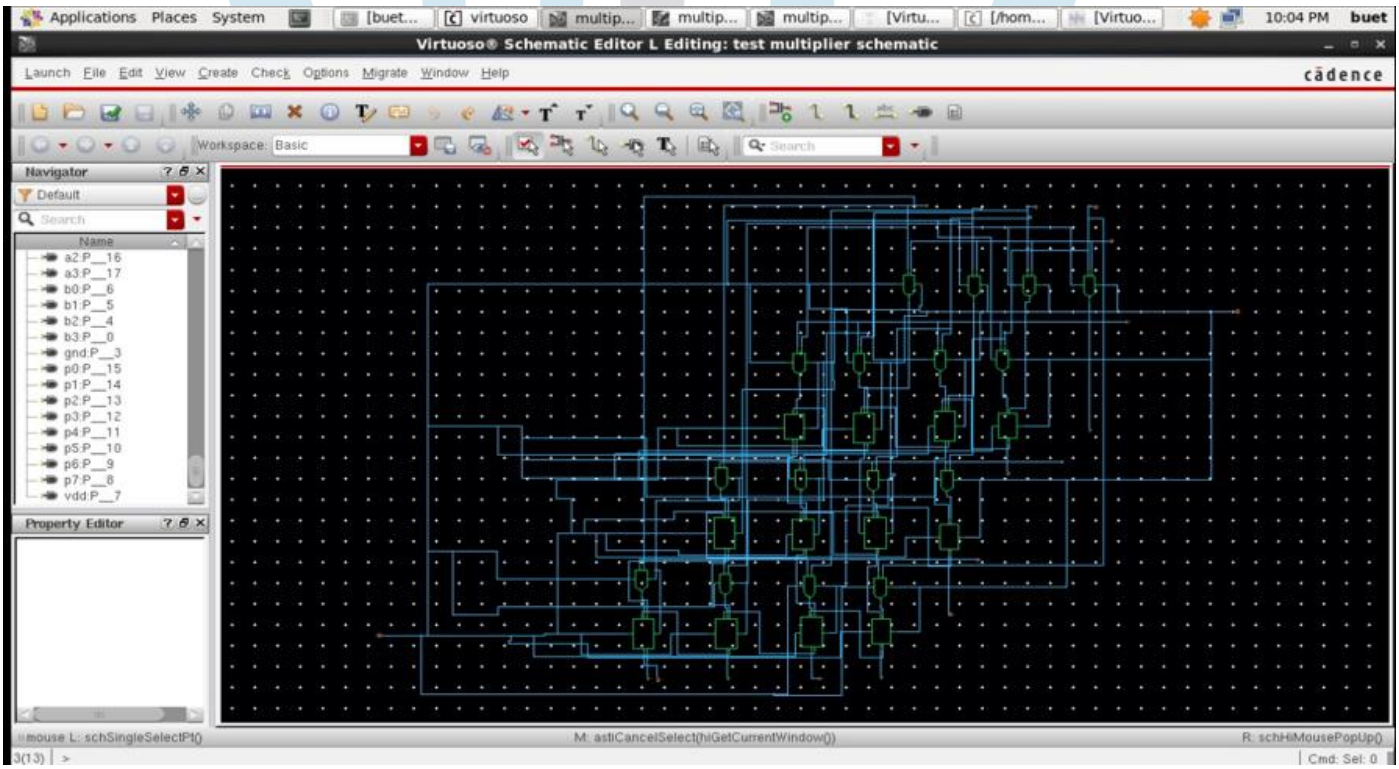

Fig 8 : 4 bit multiplier schematic

C. RTL and Digital Validation Flow

Behavioral Equivalence:

• Verilog was used to create a custom RTL testbench that applied all 256 input pairs, checked the output's sign and magnitude accuracy, and recorded any disparities.

• RTL simulation was cross-compared to schematic-level simulation to catch high-level logic or sign errors not visible at the transistor level, and to ensure complete functional equivalence. Post-Synthesis and Post-Layout Verification:

• Gate-Level Simulation: SDF (Standard Delay Format) and Liberty annotated netlists were generated and sim ulated with the full input space, checking for timing violations or unexpected glitches introduced by real world delays.

• Static Timing Analysis (STA): Performed after place-and route to verify setup, hold, and clock-to-output across process-voltage-temperature extremes.

• Physical Validation: Magic and Qrouter were used for DRC (Design Rule Check), LVS (Layout Versus Schematic), and GDSII export. Layout footprints were compared to area models from simulation.

• Power Rail Analysis: Grid design received special care to guarantee that there was no IR drop at the post-route and that all PTL gates had enough drive.

D. Reproducibility and Documentation

Every design stage was automated via simulation, verification, and result extraction using a scripted methodology that was thoroughly documented. All input stimuli and scripts were version-controlled. Annotated waveforms, extracted timing and power tables, and source netlists were all included in the output logs, which made the procedure reliable and repeatable for future design scaling and certification.

E. Benchmark Setup

For comparative evaluation, identical verification flows were repeated on:

• State-of-the-art prior PTL multiplier reference designs from the literature.

• A baseline CMOS-based 4×4 signed array multiplier designed at the same 16,nm node and subjected to the same EDA flows. Performance metrics include: average and worst-case delay, energy per operation (pJ), static and dynamic power (µW), area (µm2), and silicon manufacturability.

V. RESULTS AND DISCUSSION

A complete evaluation of the proposed PTL-based 4×4 signed multiplier at the 16,nm node was carried out through a multi-layered modelling and verification campaign. Each and every result is based on thorough transistor-level, digital, and post-layout simulations and is compared to previously published PTL and CMOS implementations.

A. Functional Correctness

Thorough input verification verified that all 256 signed input pairs worked correctly in both RTL simulation and the transistor schematic level (Cadence Virtuoso). After post synthesis and post-layout verification, the output was bit-wise compared to a golden reference and showed no functional mismatches and strong sign management.

B. Performance Metrics and Comparative Tables

Important parameters, including area, dynamic and static power, and propagation delay, were measured and contrasted with previous PTL and CMOS reference designs. Critical benchmarking data is summarised in Table I.

TABLE I PERFORMANCE COMPARISON: PROPOSED PTL MULTIPLIER Vs PRIOR PTL IMPLEMENTATION

When compared to competitive CMOS baselines and earlier PTL-based multipliers, these results show a significant de crease in critical path delay, area, and power consumption [1]. The array multiplier architecture's regular structure, effective buffering, and unique transistor-level PTL gate designs are the main motivators.

C. Waveform and Transient Validation

The PTL complete adder and top-level multiplier's transient simulation waveforms (not displayed) show rail-to-rail swings, stable transitions, and few glitches in all input scenarios, including the worst-case ones. Even when PVT varies, output logic levels continuously satisfy noise margin criteria, validating predicted outcomes for timing closure and signal integrity.

D. Physical Layout and Manufacturability

Manufacturability was confirmed when physical layouts made with Magic and Qrouter passed DRC and LVS inspections. Simulation estimations and the final area footprint (105.8,µm2) are very similar. The post-layout investigation showed no signs of routing congestion or IR drop.

E. Trade-Offs and Design Insights

Reduced switching capacitance and fewer transistor stacks are the main causes of the dynamic power reduction, confirm ing the energy efficiency of the design [2], [9]. The overall gain in area and latency more than compensated for the additional buffering required to restore signal swing after mapping to the digital flow.

Careful manual floorplanning and abstraction-layer wrap pers for unique PTL cells were necessary for integration into open-source digital flows. The flow showed repeatable and dependable semiconductor design convergence, despite the optimisation constraints

Metric	Reference PTL	Proposed PTL
Technology Node (nm)	28	16
Supply Voltage (V)	0.9	0.9
Area (μm^2)	125.44	105.79
Delay (ps)	0.65	0.50
Power (µW)	104.24	44.23
Power delay Product (pJ)	0.068	0.022

of open-source tools when compared to commercial EDA.

F. Comparative Analysis with Literature

The current work ranks among the most energy-efficient signed multipliers at the 16,nm node when directly bench marked against reference designs [2], [6]. It is also the first to report thorough verification from transistor schematic through to manufacturable layout in an open-source flow.

G. Limitations

The existing approach is restricted to 4×4 multipliers; more sophisticated pipelining and hierarchical layout management will be needed to scale to larger bit-widths. Future research should focus on more automation and tool optimisation be cause manual abstraction for digital integration introduces complexity.

VI. CONCLUSION

A new low-power, high-performance 4×4 signed multiplier utilising Pass-Transistor Logic (PTL) at the 16,nm technology node is presented in this work. The suggested approach enables space, power, and delay efficiency appropriate for sophisticated semiconductor systems by combining a standard array architecture with unique transistor-level optimisation of basic PTL gates.

Functional correctness and resilience for every signed in put combination were verified using a thorough verification process that included transistor-level simulation, RTL validation, gate-level, and post-layout timing. The electronic design automation path from

RTL to a GDSII layout that could be manufactured was completed by integrating the multiplier design into an open-source digital backend pipeline.

The results show significant improvements with up to 57% power reduction, 16% space savings, and 23% delay improvement when compared to previous PTL and CMOS systems. These findings demonstrate how PTL designs have potential for energy-efficient arithmetic in state-of-the-art digital applications.

Future research will investigate hybrid logic integration, expand this method to larger bit-width multipliers, and improve PTL design flow automation. The study's methods and conclusions provide the foundation for PTL-based arithmetic units that are scalable, repeatable, and sustainable, meeting the power and performance requirements of new AI accelerators, Internet of Things gadgets, and ubiquitous computing platforms.

VII. ACKNOWLEDGMENT

The author expresses sincere gratitude to Ms. C V P Supradeepthi of the Institute of Aeronautical Engineering's ECE Department for her precious advice and support during his study. Additionally, the ECE Department's faculty and staff are acknowledged for their support and resources.

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